Programmes After Market Services
NME–3 Series Transceivers

Technical Information

Issue 1 10/99

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A3 Schematics/Layouts

Note: *In printed manuals all A3 drawings are located at the back of the binder*

Introduction

The CD949 has 3 Basic Operating Modes, divided into submodes:

Powerdown Mode:

In powerdown mode the complete system is switched off, it is not in service and consumes a minimum of current.

Idle Mode

normal mode

In idle mode the phone is switched on and in service (if inside network coverage).

timer mode

When Ignition is switched off the phone goes in to timermode. This means that the phones stays in idlemode for a specified time and switches itself off if no action from the user takes place.

Call Mode

HF voice call

Handsfree voice call

HS voice call

Handset voice call

Data call

Receive transmit data

Power Distribution

Power is supplied to the system via the System–Cable or SCM5 (longer one). The Figure below shows an overview of Power Supply and Protection Circuits

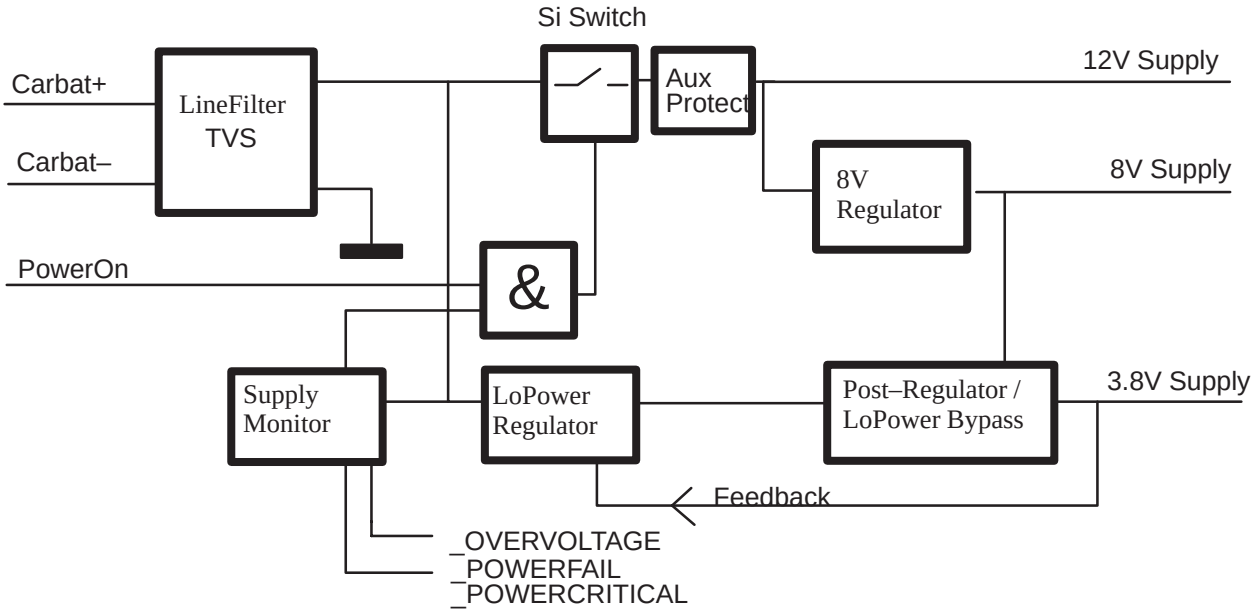


Figure 1. Power Supply Block Diagram

Table 1. Supply Voltages and Power Consumption

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
1/System 17/System	VBATT	0 5 10.8 16	 13.5	5 10.8 16 28	V/ no operation V/ reduced operation V/ nomal operation V/ no Operation
	VBATT		1.5 150	4 500 1	A Callmode mA Idle mode mA Powerdown mode

Table 2. External Signals

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
11/System	Ignition	9 0	13.5	16 0.6	V / ON V / OFF
3/System	Backlightdimming	9 13% 60	13.5	16 100% 100	V / High voltage % / Duty Cycle Hz / Frequency
4/System	Antenna motor control	V–BATT–1		VBATT 0.3 100	V / ON V / OFF mA/ Current
20/System	Car radio mute	9	1	0.3 V–BATT	V / Voicecall active V / inactive kΩ / external pullup resistance
21/System	FBUS Rx				
5/System	FBUS Tx				
23/System	MBUS				Handset
22/System	MBUS				Test/Flash
28/System	HFMic		92	843	mVrms
32/System	HF P		234	2828	mVrms
31/System	HF N		234	2828	mVrms
14/System	Line out P		70	2000	mVrms
13/System	Line out N		70	2000	mVrms
9/System	HSEar N		28	802	mVrms
10/System	HSEar P		28	802	mVrms
26/System	HSMicN		87	790	mV Microphone – to microphone +
25/System	HSMicP		87	790	mV Microphone + to microphone –
8/System	HS Powerbutton				
1/Data	DCD	+/– 3.3		+/– 15	V/ inactive V /active
2/Data	Received Data (output)	+/– 3.3		+/–15	V / binary state 1 V / binary state 0
3/Data	transmitted data (input	+/– 3.3		+/– 15	V/ binary state 1 V/ binary state 0
4/Data	DTR	+/– 3.3		+/– 15	V / inactive V / active
5/Data	GND		0		V/ reference ground
6/Data	DSR	+/– 3.3		+/– 15	V / inactive V/ active

Table 2. External Signals (continued)

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
7/Data	RTS	+/– 3.3		+/– 15	V / inactive V/ active
8/Data	CTS	+/– 3.3		+/– 15	V / inactive V/ active
9/Data	RI	+/– 3.3		+/– 15	V / inactive V/ active

Protection Circuits

Power is first filtered and protected agains Voltages>30V and Reverse Voltage. The Supply Monitor switches off the 12V Supply via Si–Switch at supply Voltages > 16.25V. Aux–Protect clamps peak pulses that are not covered by the Supply Monitor. Three signals are provided to detect different supply–voltage levels by other hard– and software: _OVERVOLTAGE is active at >16.25V, _POWERFAIL at <10,9V. _POWERCRITICAL is active at a drop of more than 5% on 3.8V Supply. A LowPower Regulator is used for sleep power for CCONT and MAD.

Three different Voltages are used in CD949. 3.8V for CCONT (VBCCONT), 8V for RF–PREAMP, AUDIO and for VBCCONT Regulator,HS and 12V for RFPA, Audio PowerAmp. 12V and 8V can be switched by PowerOn and automatically by _OVERVOLTAGE.

Power Supply – Handset

Power is supplied to the HS via cable from RU. The Figure below shows an overview of Power Supply and Reset Circuits.

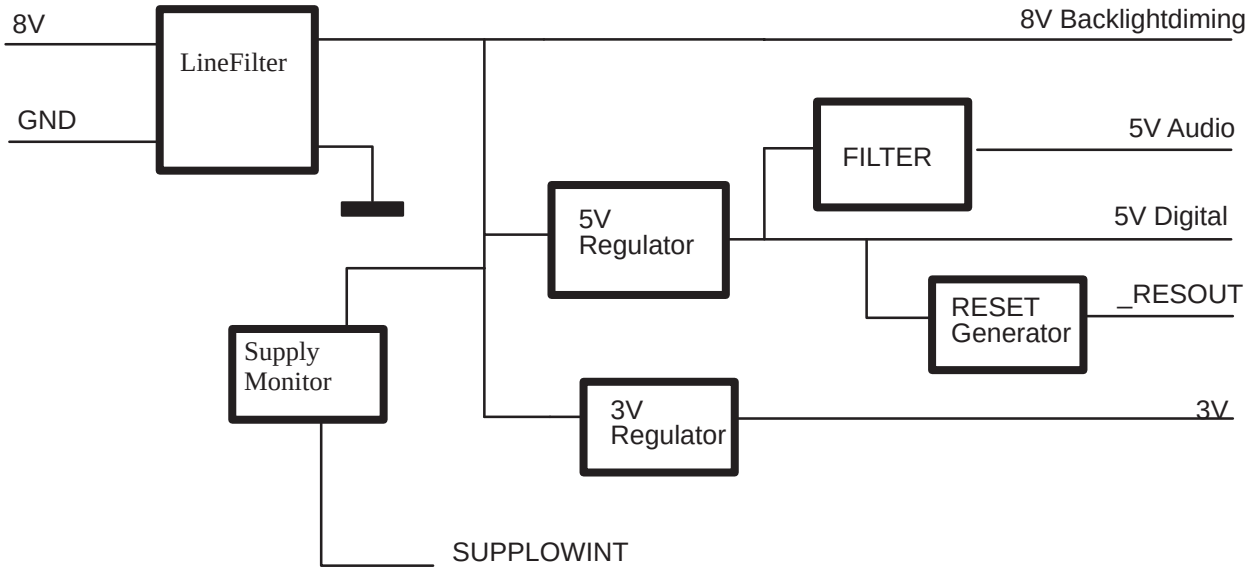


Figure 2. Power Supply Blockdiagram

External Signals and Connections

CD949 has three external connectors:
– System Connector
– Data Connector
– RF Connector

System Connector

Table 3. External Signals

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
19/System	Ignition	9 0	13.5	16 0	V / ON V / OFF
3/System	Backlightdimming	9 13% 60	13.5	16 100% 100	V / High voltage % / Duty Cycle Hz / Frequency
4/System	Antenna motor control	9		VBATT 0.3 100	V / ON V / OFF mA/ Current
20/System	Car radio mute	9	1	0.3 16	V / Voicecall active V / inactive kΩ / external pullup resistance
21/System	FBUS Rx				
5/System	FBUS Tx				
23/System	MBUS				Handset
22/System	MBUS				Test/Flash
28/System	HFMic		92	843	mVrms
31/System	HF P		234	2828	mVrms
32/System	HF N		234	2828	mVrms
14/System	Line–out P		70	2000	mVrms
13/System	Line–out N		70	2000	mVrms
9/System	HSEar N		28	802	mVrms
10/System	HSEar P		28	802	mVrms
25/System	HSMicP		87		mV Microphone + to microphone –
26/System	HSMicN		87		mV Microphone – to microphone +

Data Connector

The CD949 transceiver unit GM8B has 3 digital interfaces between the MAD and external devices. These are the data or RS232 interface, to use the transceiver as modem. The handset interface used for communication between the radiounit and the handset, and the Test and Flash interface, needed for production and after sales purposes. All of these interfaces are implemented using the M– and F–Bus coming from the MAD.

Table 4. Data interface Spec RS 232

Signal name	Signal-type	electrical spec	Pinnum-ber	Notes
RS232 DCD	Output	+– 3,3V .. 15V	PIN 1	Handshake: Data Carrier Detect
RS232 TX	Output	+– 3,3V .. 15V	PIN 2	RS 232 interface for dataaplications and remo-tecontrol aplications using advanced At–com-mandset
RS232 RX	Input	+– 3,3V .. 15V	PIN 3	RS 232 interface for dataaplications and remo-tecontrol aplications using advanced At–com-mandset
RS232 DTR	Input	+– 3,3V .. 15V	PIN 4	Handshake: Data Terminal ready
GND	Power-supply	0V DC GND	PIN 5	
RS232 DSR	Output	+– 3,3V .. 15V	PIN 6	Handshake: Data Set Ready
RS232 RTS/	Input	+– 3,3V .. 15V	PIN 7	handshake: ready for receiving
RS232 CTS	Output	+– 3,3V .. 15V	PIN 8	handshake: Clear to send
RI	Output	+– 3,3V .. 15V	PIN 9	handshake: Ring Indication

All Signals converted from RS232 level to 2.8V with a normal RS232 Levelconverter which has an own chargepump. All handshake signals are controlled by the MAD via the Row/Col pins originally used for the keyboard . The RX and TX signals are connected to the F–Bus that is shared with the Testinterface.

SIM Connector RU

Table 5. SIM–Card interface

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	VCC	4.5 2.7		5.5 3.3 10 6	V / supply voltage for 5V cards V / supply voltage for 3V cards mA / supply current for 5V cards mA / supply current for 3V cards
2	Reset	0 4.3 0 2.4		0.6 VCC 400 0.6 3 400	V / low voltage for 5V cards V / high voltage for 5V cards µs / rise and falltime V / low voltage for 3V cards V / high voltage for 3V cards µs / rise and falltime
3	CLK	0 3.5 0 2.1 45 1	 3.25	0.5 5 0.6 3 9% of period 9% of period 50 50 55 5	V / low voltage 5V cards V / high voltage 5V cards V / low voltage 3V cards V / high voltage 3V cards ns / risetime 5V cards ns / falltime 5V cards ns / risetime 3V cards ns / falltime 3V cards % / duty cycle MHz / clock frequency
4	N.C.				reserved for future use
5	GND				ground

Table 5. SIM–Card interface (continued)

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
6	VPP	4.5 2.7		5.5 3.3	V / programming voltage idle state 5V cards V / programming voltage idle state 3V cards
7	I/O	–0.3 3.5 0 3.8 –0.3 2.1 0 2.1		0.8 5.3 0.4 5 0.6 3.3 0.4 3 1 1	V / input low voltage 5V cards V / input high voltage 5V cards V / output low voltage 5V cards V / output high voltage 5V cards V / input low voltage 3V cards V / input high voltage 3V cards V / output low voltage 3V cards V / output high voltage 3V cards µs / risetime µs / falltime
8	N.C				reserved for future use

SIM Connector HS

Table 6. SIM–Card interface

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	VCC	4.5 2.7		5.5 3.3 10 6	V / supply voltage for 5V cards V / supply voltage for 3V cards mA / supply current for 5V cards mA / supply current for 3V cards
2	Reset	0 4.3 0 2.4		0.6 VCC 400 0.6 3 400	V / low voltage for 5V cards V / high voltage for 5V cards µs / rise and falltime V / low voltage for 3V cards V / high voltage for 3V cards µs / rise and falltime
3	CLK	0 3.5 0 2.1 45 1	 3.25	0.5 5 0.6 3 9% of period 9% of period 50 50 55 5	V / low voltage 5V cards V / high voltage 5V cards V / low voltage 3V cards V / high voltage 3V cards ns / risetime 5V cards ns / falltime 5V cards ns / risetime 3V cards ns / falltime 3V cards % / duty cycle MHz / clock frequency
4	N.C.				reserved for future use
5	GND				ground
6	VPP	4.5 2.7		5.5 3.3	V / programming voltage idle state 5V cards V / programming voltage idle state 3V cards
7	I/O	–0.3 3.5 0 3.8 –0.3 2.1 0 2.1		0.8 5.3 0.4 5 0.6 3.3 0.4 3 1 1	V / input low voltage 5V cards V / input high voltage 5V cards V / output low voltage 5V cards V / output high voltage 5V cards V / input low voltage 3V cards V / input high voltage 3V cards V / output low voltage 3V cards V / output high voltage 3V cards µs / risetime µs / falltime
8	N.C				reserved for future use

Internal Signals and Connections

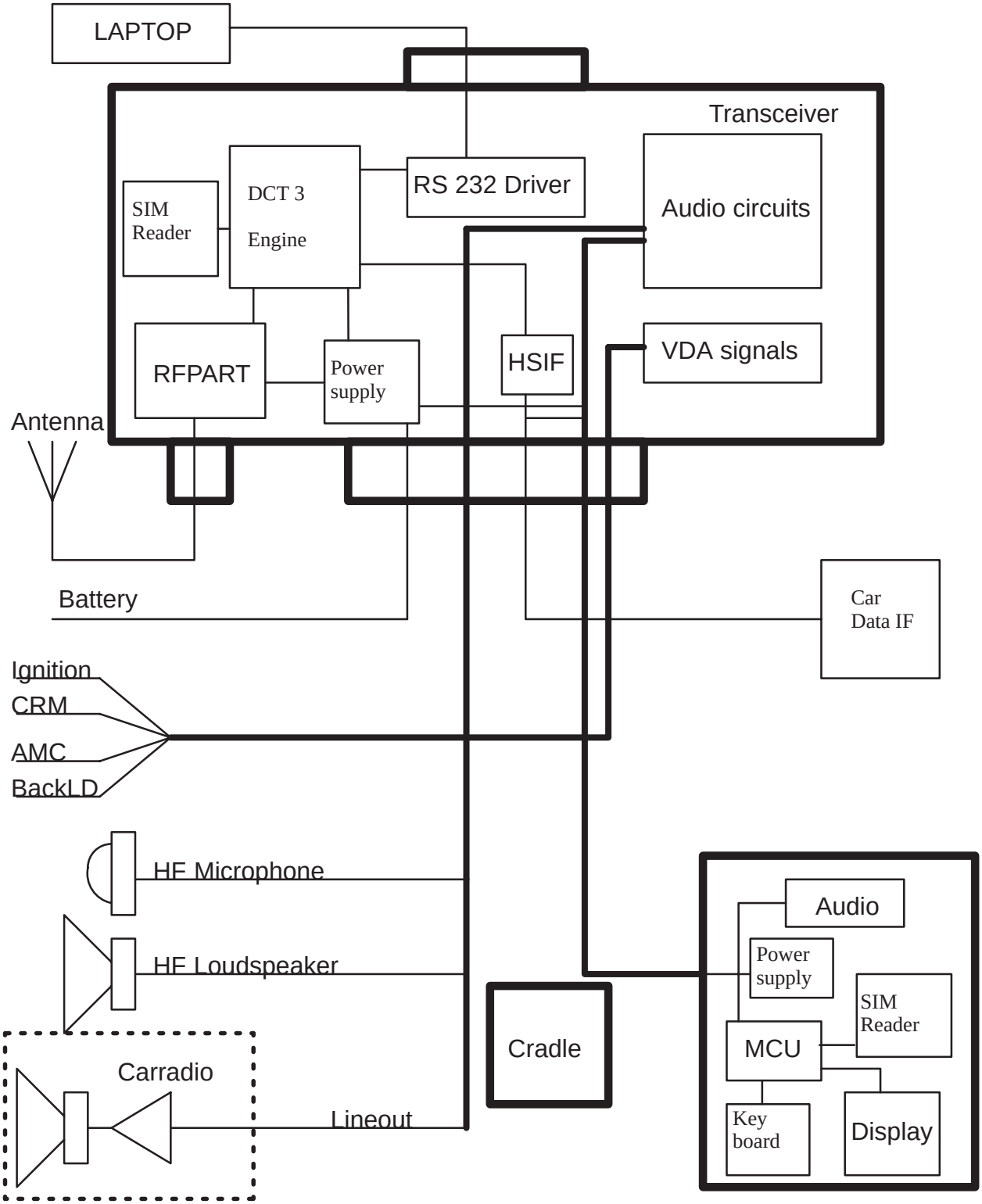


Figure 3.

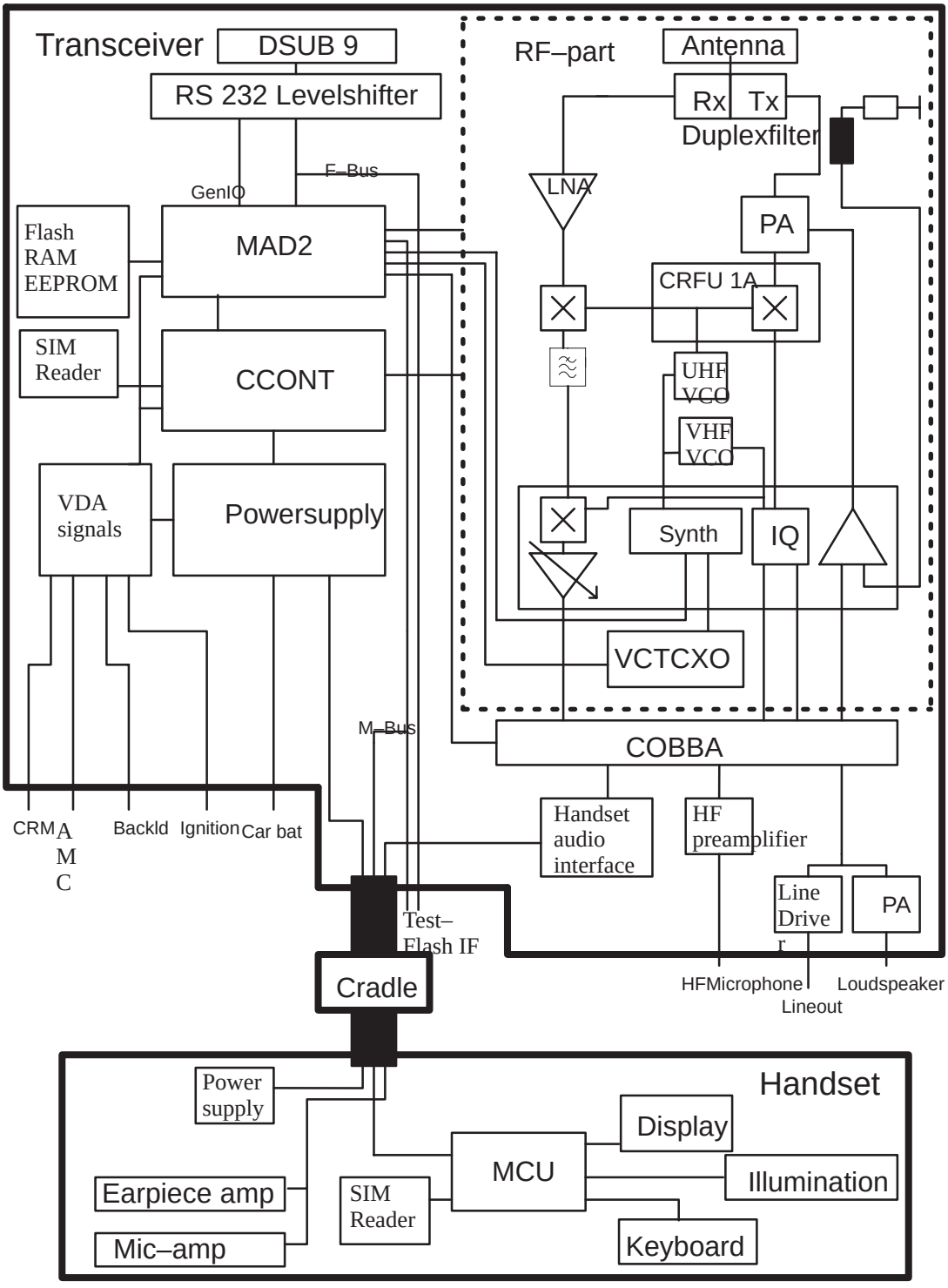


Figure 4. CD 949 System overview

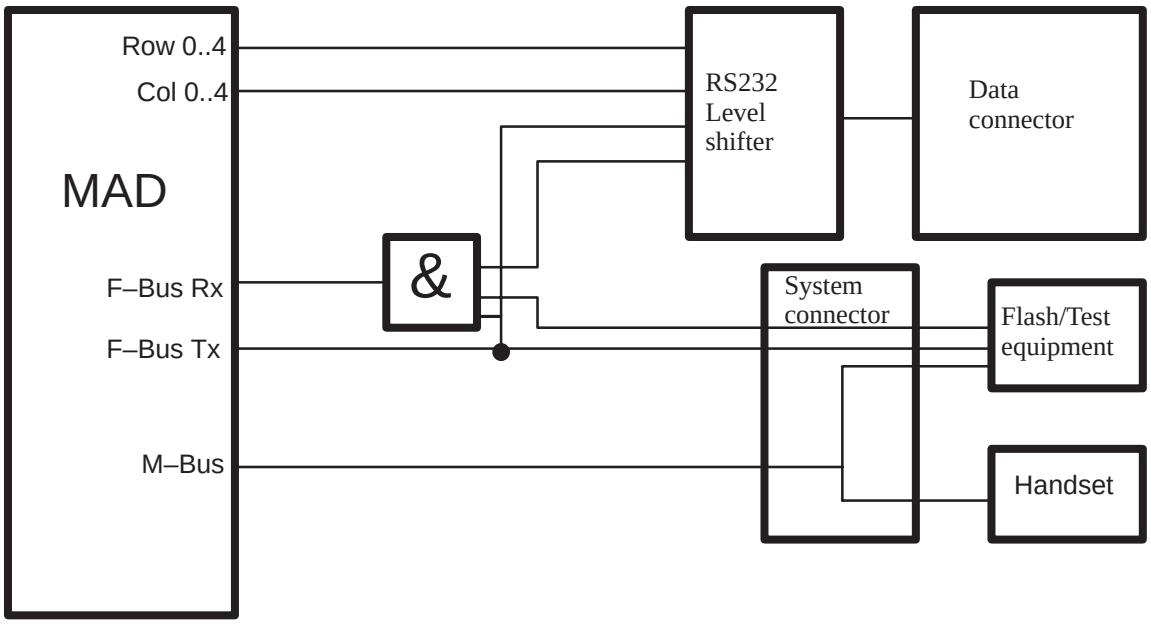


Figure 5. Digital interface in GM8B

SYS Conn Block Conections

Audio Block Connections

The Cobba has to functions AD/DA converters for the RF–BB interface. Codecs for the Audio interface. The RF–BB interface is used implemented in the same way it is implemented in HD940. The Cobba audio interface is used different to the handys. The Inputs and outputs for HS–use, which are normally connected directlly to the Microphone and the earpiece are connected to the Handset via balanced drivers and receivers. The Handsfree input and output is connected to the analog HFanalog audio parts on the RU PCB via Balanced lines as well.

Audio Connection to Handset

The audio interface to the HS will not be reused from CD 940. It consists of balanced audiolines from Cobba to Earpiece and from HS Microphone to Cobba.

Table 7. Audio levels for HS

Signal name	Nominal value	Maximum value	Notes
HS EARP/EARN	17,5 mV_{RMS}	501 mV_{RMS}	This is the balanced signal level at the HS
HS MICP/MICN	87 mV_{RMS}	790 mV_{RMS}	This is the balanced signal level at the HS/ RU

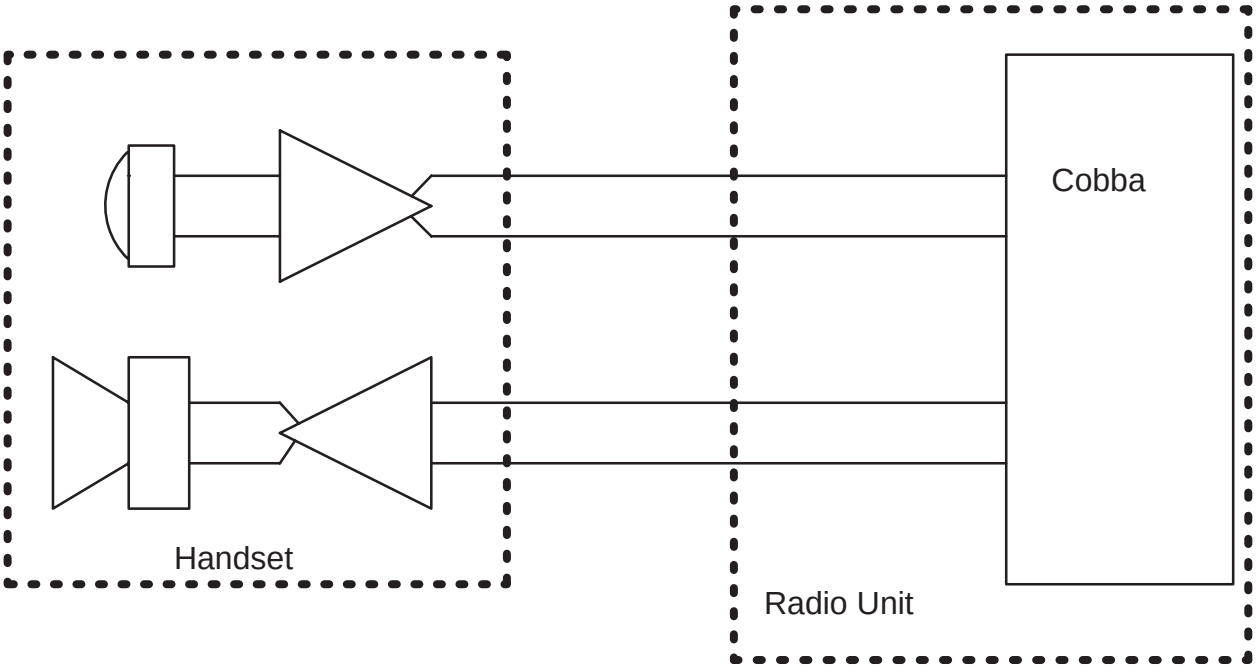


Figure 6. HS audio interface

Handsfree Audio Path

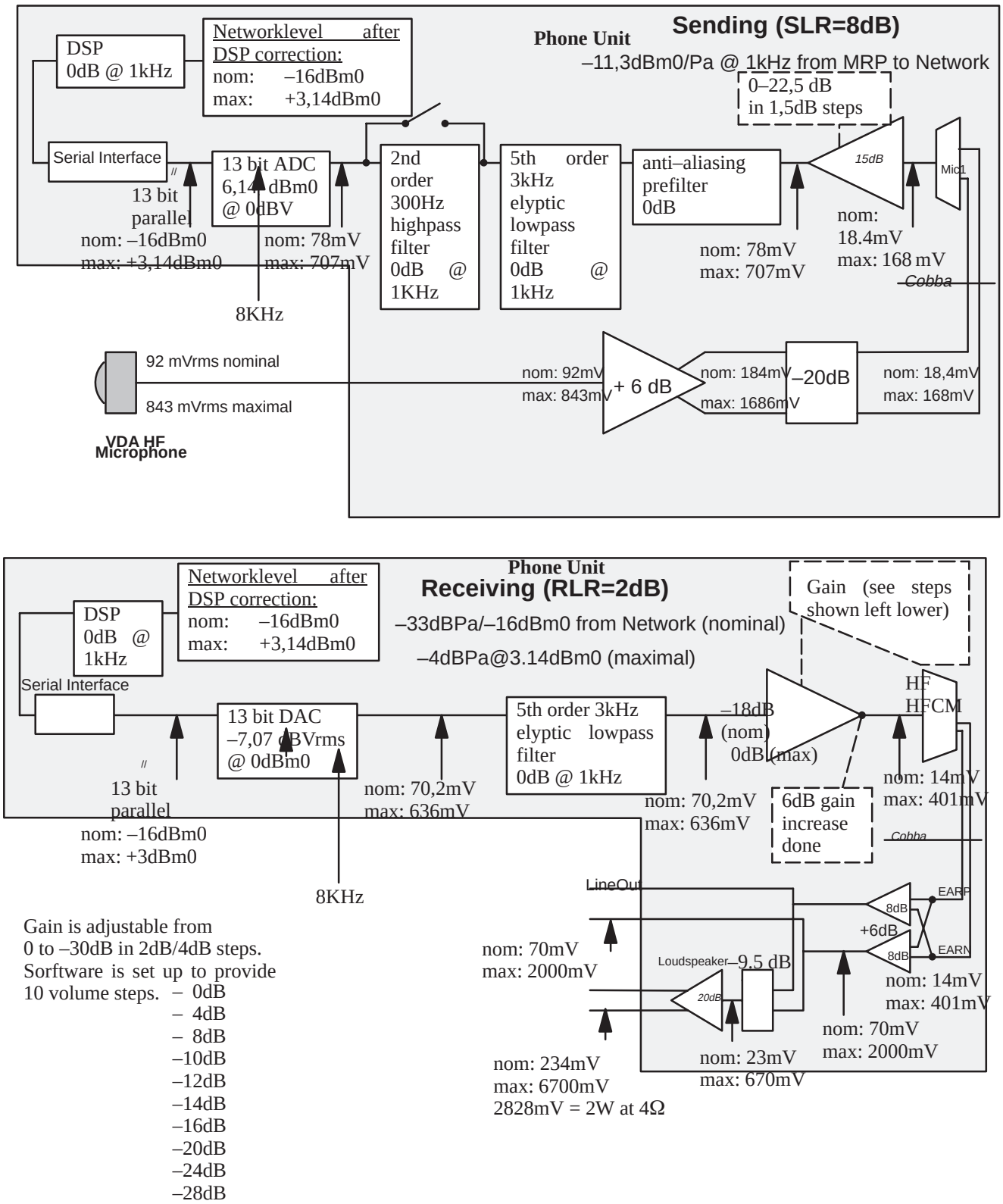
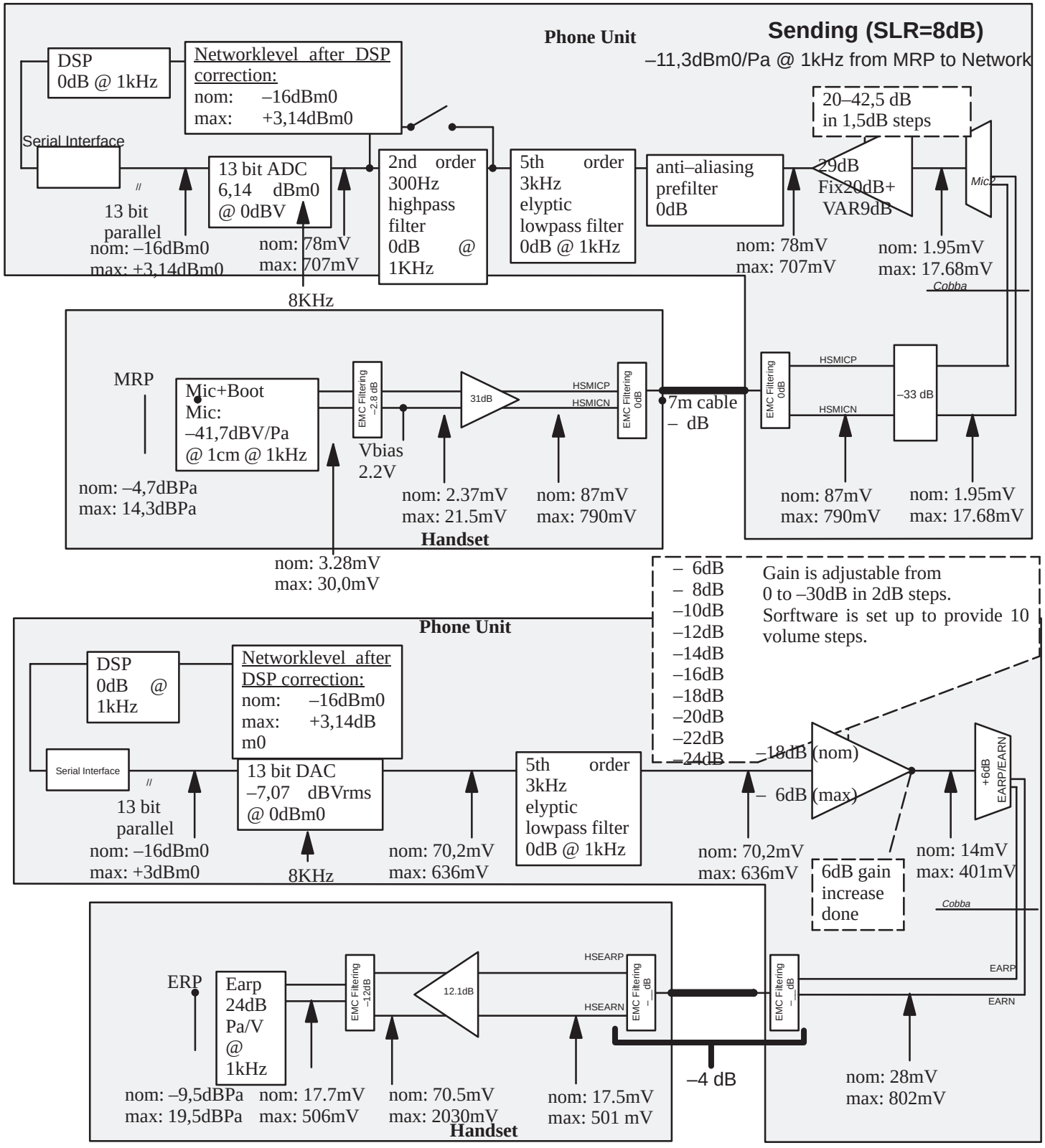


Figure 7. Audio Paths for Hands–Free

Handset Audio Path



Receiving (RLR=2dB)
6,5dBPa/0dBm0 from Network to ERP (nominal)
19,5dBPa@3,14dBm0 (maximal)

Figure 8. Audio Path – Hand–Set

Handsfree Loudspeaker

According to VDA at has to be suitable to drive 4Ω Loudspeakers with a maximumpower of 5W. When checking the offical requirements for the response of the loudspeakerpart, we see that we need to have at 1,5W Audiopower , if the sensitivity is as specified in CD949 acoustical components. We are using a bridged Audio Amp. The requirements for the Loudspeaker are shown below:

Table 8. Loudspeakeroutput

Parameter	Value	Note
Loadimpedance	3Ω– 5Ω	
Power at 1% THD	1,5W	
minimum drive capacitance	10 nF	
Frequency response	300 Hz – 6,8 kHz	
Total Powersupply rejection ratio	> 60 dB	

Handsfree Microphone

Specification for microphone input

First stage in the CD949 microphone path is an active microphone. This is needed to get a good signal to noise ration on the long cable between microphone and CD949 radio unit. The electrical specification for the microphone (according VDA) could be seen in the table below.

1. 8V Biasvoltage
2. only two Pins
3. 10 kΩ minimum load
4. at P=74dB,1 khz and 30cm distance it has to deliver 190 mV_{PP} with a distortion of less then 1%
5. more then 15 dB dynamic range
6. Flat frequency response from 300 Hz to 4 khz +– 1 dB
7. signal to Noise ratio of more then 50 dB at 1% distortion limit
8. mountable on sunscreen and at chassis of the Car
9. Possibility to drive 7m microphone cable

To interface this microphone, the CD949 radio unit has a low noise power supply The input stage of CD949 has to have an input impedance of >20 kΩ.

Table 9. Specification for Microphone interface

Parameter	Value	Notes
Bias voltage	8V +– 10%	<10 mV ripple max
Bias source impedance	>300 Ω	
Load resistance	>10 kΩ	
AF level	190 mV_{pp}	at 1khz P=74 dB >1% distortion 15 dB dynamic range

The specifications for the line out is that it will be a balanced driver with the capability of driving high capacitance loads, which are results of long cables and EMC filtering. The load impedances and voltage levels are defined and listed in the table below.

Table 10. Line out

Parameter	Value	Note
Loadimpedance	>1k Ω	
Outputlevel	max 2000mV RMS nom 70mV RMS	
minimum drive capacitance	1 nF	
Frequency response	300 Hz – 6,8kHz	only analog Amplifiers

The Interface signals between the Baseband and the RF section of the CD949 are shown in the following table below. On physical board level the Baseband supplies voltages from CCONT Asic to seperate RF sub blocks. The maximum values specified for the digital signals in the table is the absolute max. value from the RF interface point of view.

Table 11. AC and DC Characteristics of RF baseband signals

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
VPA	Unreg. car battery voltage protected against overvoltage	RF–PA	Voltage	10.5	13.0	16.5	V	Supply voltage for RF (controlled with VTX), and TX Interstage Amplifier (current in TX slot)
			Current		3150	4500	mA	
VREF	CCONT	PLUSSA	Voltage	1.478	1.5	1.523	V	Reference voltage for PLUSSA and CRFU1a
			Current			100	uA	
			Source resistance		10		ohm	
VRX1	CCONT (VR5)	PLUSSA (32mA),	Voltage	2.7	2.8	2.85	V	Supply voltage for RF Receiver (Plussa RX section)
			Current		32		mA	
VRX2	CCONT (VR2)	LNA (25mA), IFAmp (25mA) (VRX1)	Voltage	2.7	2.8	2.85	V	Supply voltage for RF Receiver (LNA, IFAMPLIFIER)
			Current		50		mA	

Table 11. AC and DC Characteristics of RF baseband signals (continued)

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
VXO	CCONT (VR1)	VCTCXO (2mA), Buffer (5mA)	Voltage	2.7	2.8	2.85	V	Supply voltage for RF VCTCXO and buffer stage to Plussa if required
			Current		7		mA	
VSYN	CCONT (VR3)	PLUSSA (19mA)	Voltage	2.7	2.8	2.85	V	Supply voltage for RF Synthesizer Digital Part (VP1, VP2, VDD)
			Current		19		mA	
VVCO	CCONT (VR4)	UHFVCO (10mA), VHFVCO (5mA), CRFU1a (7mA), buffer (10mA)	Voltage	2.7	2.8	2.85	V	Supply voltage for RF VCOs including a buffer and VDDSTBYBIAS and VDDSTBYLB pins of the CRFU1a
			Current		32		mA	
VCP	CCONT (V5V)	PLUSSA Charge Pumps	Voltage	4.8	5.0	5.2	V	Supply voltage for RF Charge Pumps on the Plussa ASIC
			Current		4		mA	
V8PA	VBBDIG	Logic circuits PA	Voltage	7.60	8.0	8.40	V	Supply voltage for RF PA logic circuits (controlled with TXP), Op-Amp for PA biasing
			Current		40	60	mA	
VTX	CCONT (VR7)	PLUSSA CRFU1a	Voltage	2.7	2.8	2.85	V	Supply voltage for RF TX parts on Plussa and CRFU1a
			Current		72		mA	
VXOPWR	MAD	CCONT	Logic high ”1”	2.0		2.85	V	VR1, VR6 in CCONT ON
			Logic low ”0”	0		0.8	V	VR1, VR6 in CCONT OFF
			Current			0.1	mA	
			Timing inaccuracy			10	us	
SYNPWR	MAD	CCONT	Logic high ”1”	2.0		2.85	V	VR3, VR4 in CCONT ON
			Logic low ”0”	0		0.8	V	VR3,VR4 in CCONT OFF
			Current			0.1	mA	
RXPWR	MAD	CCONT	Logic high ”1”	2.0		2.85	V	VR2, VR5 in CCONT ON
			Logic low ”0”	0		0.8	V	VR2, VR5 in CCONT OFF
			Current			0.1	mA	
TXPWR	MAD	CCONT RF–part	Logic high ”1”	2.0		2.85	V	VR7 in CCONT ON
			Logic low ”0”	0		0.8	V	VR7 in CCONT OFF
			Current			0.1	mA	Switches V8PA ON/ OFF

Table 11. AC and DC Characteristics of RF baseband signals (continued)

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
PDATA0	MAD	LNA	Logic high ”1”	2.0		2.85	V	Nominal gain in LNA
			Logic low ”0”	0		0.8	V	Reduced gain in LNA
			Current			0.1	mA	
SENA	MAD	PLUSSA	Logic high ”1”	2.0		2.85	V	PLL enable
			Logic low ”0”	0		0.8	V	
			Current			50	uA	
			Load capacitance			10	pF	
SDATA	MAD	PLUSSA	Logic high ”1”	2.0		2.85	V	Synthesizer data
			Logic low ”0”	0		0.8	V	
			Load impedance	10			kohm	
			Load capacitance			10	pF	
			Data rate frequency		3.25		MHz	
			Databits S10–S14		10101			
SCLK	MAD	PLUSSA	Logic high ”1”	2.0		2.85	V	Synthesizer clock
			Logic low ”0”	0		0.8	V	
			Load impedance	10			kohm	
			Load capacitance			10	pF	
			Data rate frequency		3.25		MHz	
AFC	COBBA	VCTCXO	Voltage	0.046		2.254	V	Automatic frequency control signal for VC(TC)XO
			Resolution	11			bits	
			Load resistance (dynamic)	10			kohm	
			Load resistance (static)	1			Mohm	
			Noise voltage			500	uVrms	10...10000Hz
			Settling time			0.5	ms	
RFC	VCTCXO	MAD	Frequency		13		MHz	High stability clock signal for the logic circuits
			Signal amplitude	0.5	1.0	2.0	Vpp	
			Load resistance	10			kohm	
			Load capacitance			10	pF	
RXIP/ RXIN	PLUSSA	COBBA	Output level		50	1344	mVpp	Differential RX 13 MHz signal to baseband
			Source impedance			tbd.	ohm	
			Load resistance		1		Mohm	
			Load capacitance			tbd.	pF	

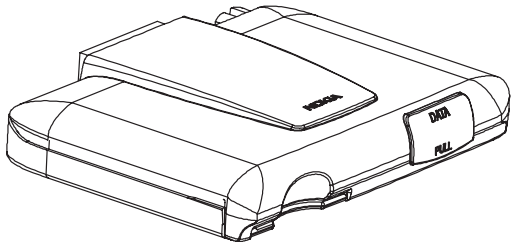
Table 11. AC and DC Characteristics of RF baseband signals (continued)

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
TXIP/ TXIN	COBBA	PLUSSA	Differential voltage swing	1.022	1.1	1.18	Vpp	Differential in–phase TX baseband signal for the RF modulator
			DC level	0.784	0.8	0.816	V	
			Differential offset voltage (corrected)			+/– 2.0	mV	
			Diff. offset voltage temp. dependence			+/– 1.0	mV	
			Source impedance			200	ohm	
			Load resistance	40			kohm	
			Load capacitance			10	pF	
			DNL			+/– 0.9	LSB	
			INL			+/–1	LSB	
			Group delay mis-smatch			100	ns	
TXQP/ TXQN	COBBA	PLUSSA	Differential voltage swing	1.022	1.1	1.18	Vpp	Differential quadrature phase TX baseband signal for the RF modulator
			DC level	0.784	0.8	0.816	V	
			Differential offset voltage (corrected)			+/– 2.0	mV	
			Diff. offset voltage temp. dependence			+/– 1.0	mV	
			Source impedance			200	ohm	
			Load resistance	40			kohm	
			Load capacitance			10	pF	
			Resolution	8			bits	
			DNL			+/– 0.9	LSB	
			INL			+/–1	LSB	
			Group delay mis-smatch			100	ns	
TXP	MAD	PLUSSA	Logic high ”1”	2.0		2.85	V	Transmitter power control enable
			Logic low ”0”	0		0.8	V	
			Load Resistance	50			kohm	
			Load Capacitance			10	pF	
			Timing inaccuracy			1	us	

Table 11. AC and DC Characteristics of RF baseband signals (continued)

Signal name	From	To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
TXC	COBBA	PLUSSA	Voltage Min	0.12		0.18	V	Transmitter power control
			Voltage Max	2.27		2.33	V	
			Vout temperature dependence			10	LSB	
			Source impedance active state			200	ohm	
			Source impedance power down state	high Z				
			Input resistance	10			kohm	
			Input capacitance			10	pF	
			Settling time			10	us	
			Noise level			500	uVrms	0...200 kHz
			Resolution	10			bits	
			DNL			+/–0.9	LSB	
			INL			+/– 4	LSB	
			Timing inaccuracy			1	us	
RXC	COBBA	PLUSSA	Voltage Min	0.12		0.18	V	Receiver gain control
			Voltage Max	2.27		2.33	V	
			Vout temperature dependence			10	LSB	
			Source impedance active state			200	ohm	
			Source impedance power down state	grounded				
			Input resistance	1			Mohm	
			Input capacitance			10	pF	
			Settling time			10	us	
			Noise level			500	uVrms	0...200 kHz
			Resolution	10			bits	
			DNL			+/–0.9	LSB	
			INL			+/– 4	LSB	
LOOP	MAD2 (DSP GEN-OUT1)	Power Detector	Logic high ”1”	2.0		2.85	V	Low impedance mode (High Power level range (200mW...8W))
			Logic low ”0”	0		0.8	V	High impedance mode (Low Power level range (3mW...126mW)
			Current			0.1	mA	

Transceiver (NME–3)



Baseband

This chapter of the document describes the baseband module of the DCT3 engine used in CD949. The Baseband architecture is basically similar to DCT2 GSM phones. The DCT3 differs from DCT2 in the integration level of the baseband. In DCT3 the MCU, the system specific ASIC and the DSP are integrated in one ASIC called MAD. This chip takes care of all the signal processing and operation controlling tasks of the phone.

The baseband architecture supports a power saving mode called ”sleep mode”. This sleep mode shuts off the VCTCXO, which is used as system clock for RF and baseband. During the sleep mode the system runs from a 32khz crystal. The phone is woken up by a timer running from this 32khz clock supply. The sleeping time is determined by some network parameters. The sleep mode is entered when MCU and DSP are in stand by mode and the normal VCTCXO clock has been switched off.

The nominal supply voltage for the baseband part of the engine is 2.8V.

Functional Description

The Baseband functions are controlled by the MAD ASIC, which consists of a MCU a system ASIC and a DSP. The GSM/PCN specific ASIC is named MAD2. All the MAD ASICs contains the same core processors and similiar building blocks, but they differ from each other in system specific functions, pinout and package types.

MAD2 contains the following blocks:

– ARM RISC processor with both 16 bit instruction set (THUMB mode) and 32 bit instruction set (ARM mode)

– TI LEAD DSP core with peripherials:

– API (Arm Port Interface Memory) for MCU–DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting.

– Serial Port (connetion to PCM)

– Timer

– DSP memory

– BUSC (Bus Controller for controlling accesses from ARM to API, System logic and MCU externel Memory, both 8– and 16 bit memories)

– System Logic

– CTSI (Clock, Timing, Sleep and Interrpt control)

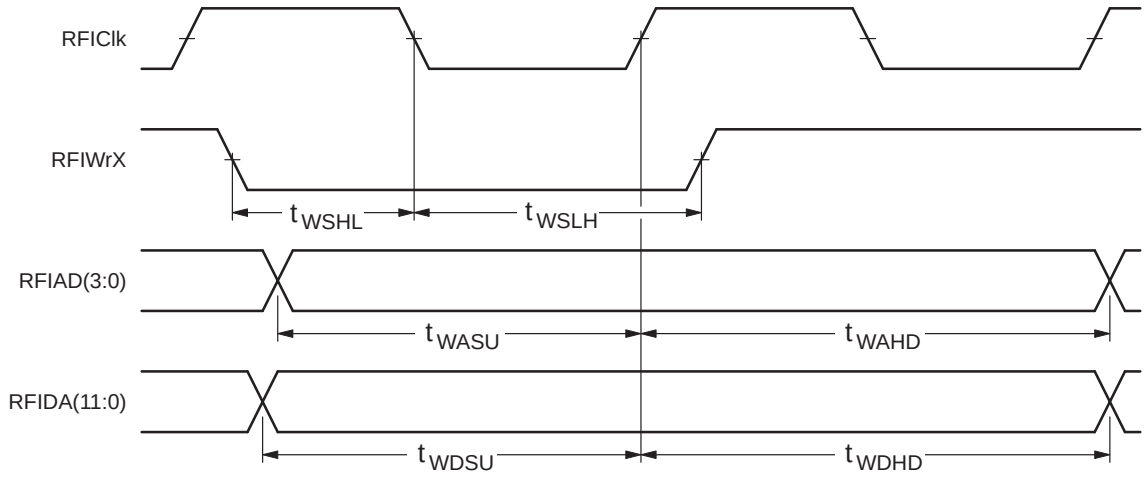


Figure 9. Write cycle timing.

Table 12. Write Cycle Timing Characteristics

Parameter	Symbol	Min	Max	unit
Write strobe active delay time	tWSHL	20	tcyc–20	ns
Write strobe inactive delay time	tWSLH	20	tcyc–20	ns
Address bus set up time	tWASU	30		ns
Address bus hold time	tWAHD	30		ns
Data bus set up time	tWDSU	30		ns
Data bus hold time	tWDHD	30		ns

CCONT for CD949

The heart of the power distrubution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories plus COBBA digital parts. There is a separate regulator for a SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT contains a real time clock function, which is powered from a RTC backup when the power supply is disconnected.

Operating mode	Vref	RF REG	VCOB-BA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	Off	On	On	On/Off

Note: *COBBA regulator is off in SLEEP mode. Its output pin may be fed from V_{BB} in SLEEP mode by setting bit RFReg(5) to '1' (default).*

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are listed the MAD control lines and the regulators they are controlling.

– TxPwr controls VTX regulator (VR5)

– RxPwr controls VRX regulator (VR2)

– SynthPwr controls VSYN_1 and VSYN_2 regulators (VR4 and VR3)

– VCXOPwr controls VXO regulator (VR1)

CCONT also generates a 1.5 V reference voltage VREF to COBBA, PLUSSA and CRFU. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

In additon to the above mentioned signals MAD includes also TXP control signals which go to PLUSSA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA to PLUSSA.

Operating mode	Vref	RF REG	VCOB-BA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	Off	On	On	On/Off

Characteristics	Condition	Min	Typ	Max	Unit
Output current VR1–VR6	Vout@2.8V			100	mA
Output current VR7 Depends on external BJT	Vout@2.8V			150	mA
Output current VR7BASE Base current limit	Vout@2.8V			–10	mA
Output current VBB On Current limit 250mA Output current VBB Sleep Current limit 5mA	Vout@2.8V Vout@2.8V			125 1	mA mA
Output voltage VR1–VR7	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Output voltage VBB	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Line regulation (not VBB)	F ≤ 10kHz, 2) VBAT>3.15V	49			dB
Line regulation (not VBB)	F ≤ 100kHz, 2) VBAT>3.15v	40			dB
Line regulation VBB	F ≤ 100kHz 2)	30			dB
Load regulation	T = 25°C		0.6	1	mV/mA
Supply current (each regulator) VR1...VR7	ON mode		I_{out}/60 +330	I_{out}/10 +540	µA
Supply current VBB	ON mode		I_{out}/60 + 250	I_{out}/10 + 400	µA
Supply current VBB	SLEEP mode		I_{out}/60 + 100	I_{out}/10 + 150	µA

Switching SIM power supply

There is a switched mode supply for the SIM–interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

Characteristics	Condition	Min	Typ	Max	Unit
Output current VR1–VR6	Vout@2.8V			100	mA
Output current VR7 Depends on external BJT	Vout@2.8V			150	mA
Output current VR7BASE Base current limit	Vout@2.8V			–10	mA
Output current VBB On Current limit 250mA Output current VBB Sleep Current limit 5mA	Vout@2.8V Vout@2.8V			125 1	mA mA
Output voltage VR1–VR7	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Output voltage VBB	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Line regulation (not VBB)	F ≤ 10kHz, 2) VBAT>3.15V	49			dB
Line regulation (not VBB)	F ≤ 100kHz, 2) VBAT>3.15v	40			dB
Line regulation VBB	F ≤ 100kHz 2)	30			dB
Load regulation	T = 25°C		0.6	1	mV/mA
Supply current (each regulator) VR1...VR7	ON mode		I_{out}/60 +330	I_{out}/10 +540	µA
Supply current VBB	ON mode		I_{out}/60 + 250	I_{out}/10 + 400	µA
Supply current VBB	SLEEP mode		I_{out}/60 + 100	I_{out}/10 + 150	µA

CCONT use in CD949

The CCONT is the Powersupply asic in the DCT3 architecture. The main difference between the HD940 and the CD949 CCONT application is that in CD949 all the charging and battery related signals are disabled. The EAD ADC input is used for backlightdimming. The PowerOnX pulse for the CCONT is generated by 3 different sources

1. Ignition gets High
2. The Powerbuttom is pressed
3. The Supplyvoltage comes up from below 3.8V
4. PURX gets low caused by softwarecrash

Handset interface

The handset interface is implemented using the M–Bus. M–Bus is used for Test puposes as well, but since M–Bus is a multipointbus there is no problem in using M–Bus for multiple purposes.

For Test and Flash purposes F– and M–Bus are directly connected from the MAD to the systemconnector. This enables us to use the common Test and Flash utilities used for HD 941 and HD 943 for CD949 in the same way.

Multiplexing the Busses

The M–Bus is a multipoint bus, that could be used for both purposes (Test/Flash and Handset) without any restrictions. The F–Bus is designed as a point to point bus, so that it is not possible to connect it to 2 parties (Data–If and Test IF) directlly. In CD949 it is implemented in a way that the F–Bus TX from the MAD is going to the Data interface and the Test interface. The Signals coming from the 2 interfaces are combined by a AND–gate before they are going to the F–BUS RX. This means that you could try to use both interfaces at the same time without any risk of damage to any device, but it is not possible to make data transfer via the RS232, will using the F–Bus for test or trace purposes. This is no major drawback, because when you are flashing or aligning the product in the factory, you are not using the data interface, and the enduser who need s the Data interface is not touching the test interface at all.

SIM Card in RU

Due to the fact that we are reusing the CD745 mechanical parts we have also to reuse the CD745 SIM card reader.

Power up/Power down procedure

In the gm8b the CCONT is acting as Reset and Powercontrol Master, as well as as watchdogtimer. In a normal handportable DCT3 phone the main powerupprocedure works as following: The user presses the powerbutton, this signal is delivered to the CCONT via its poweronxpin. If this signal is valid for more then 50mS the CCONT turns on PURX in order to RESET the MAD and handover the control to the MAD. When the phone is switched off or the software crashes the MAD is no longer reseting the CCONTs watchdogtimer , the watchdogtimer gives an alert, CCONT switches PURX off and puts the phone into sleepmode.

In case of a handy its O.K. when the user has to switch on the phone again after a softwarecrash, in a carphone (without a handset ??) he won’t even realise that there is a problem, so this behaviour is not acceptable.

Description of gm8b Powerup/Powerdown behaviour

In a carphone there are 2 sources that wakeup the system in a normal situation:

1. Ignition is turned on
2. The User presses the Powerbutton

In both situations the phone has to stay in Power On status as long as the Userpresses the Powerbutton again or Ignition is turned OFF. It should not be switched off when the software crashed

To gauranty this behaviour, we have added several extra circuits around CCONT. In gm8b are 4 events that generate a 100mS pulse on poweronx and switch on CCONT.:

1. Ignition is switched ON
2. Powerbutton is pressed
3. The Carbatteryvoltage comes up from below 3.8V (Brownout).
4. PURX goes down caused by a software crash

In order to decide if the PURX is going low because of a Softwarecrash, or because of a regular Shutdown, there is a Powerdown signal going from MAD to the Powercontrol unit. When the SW is initiating a Shutdown, Powerdown is set high, and the Pulse generator is disabled, and no Pulse is generated on the falling edge of PURX. The following pictures are ilustrating the Powerup/Down behaviour.

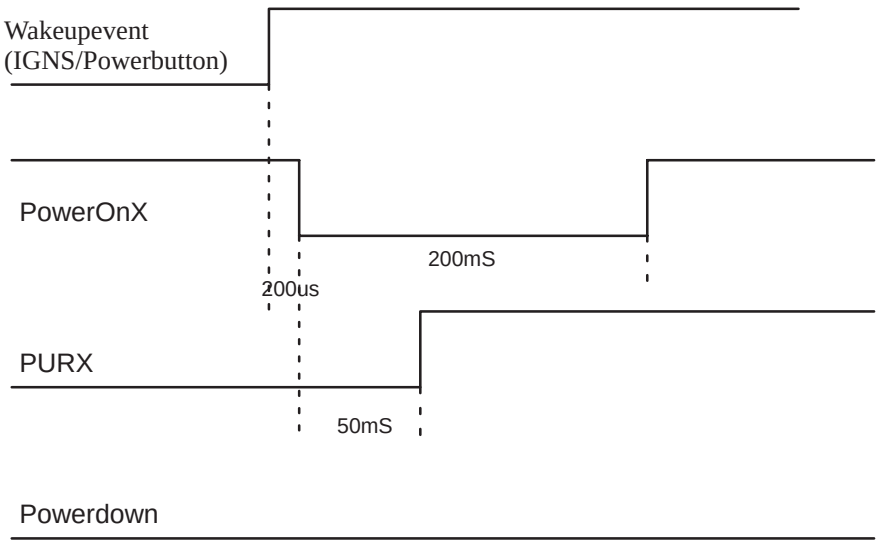


Figure 10. regular Startup

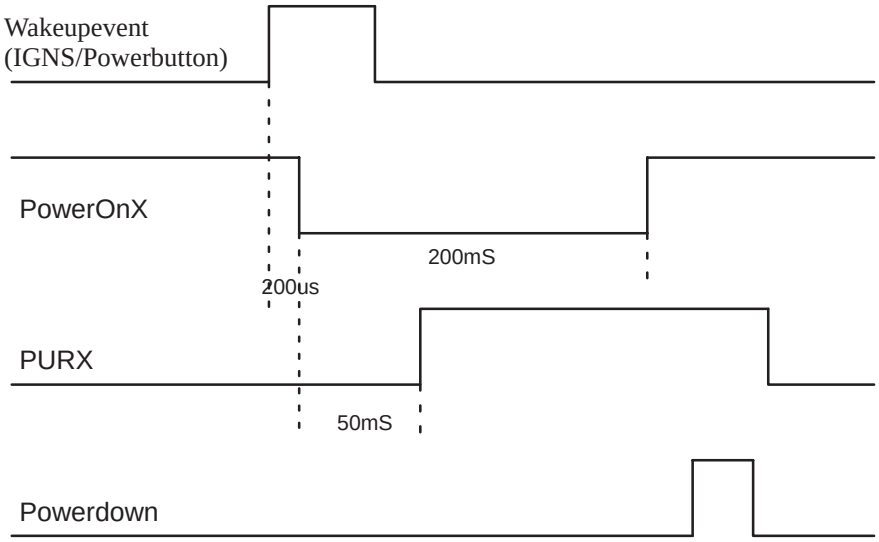


Figure 11. unvalid wakeup (ignored)

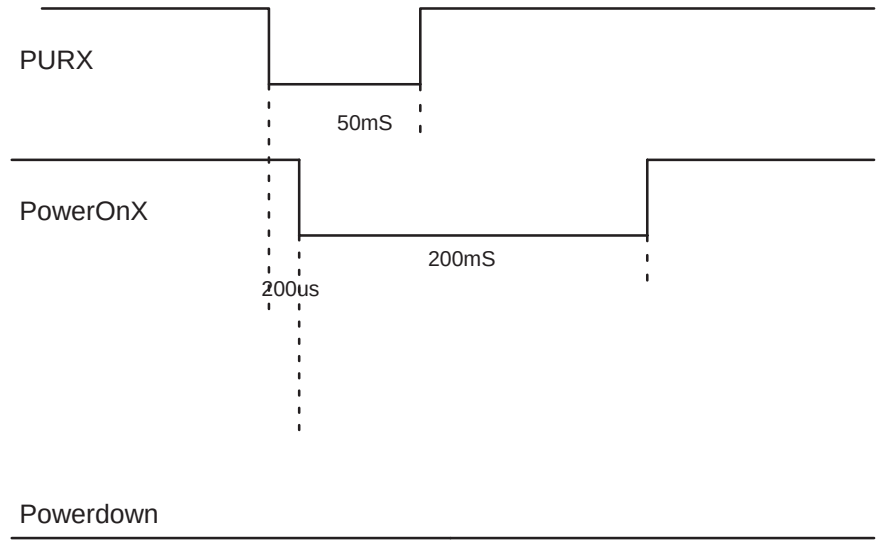


Figure 12. SW crash + Restart

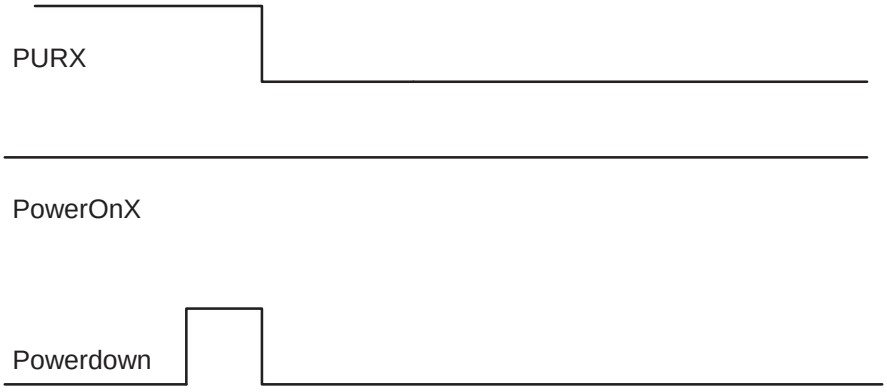


Figure 13. regular Shutdown

Description of the Brownout circuit

The CD949 transceiver is permanently connected to the Car battery which has a nominal level of 13.5 V. Since there are some systems in a car like ignition or electirical motors, it happens frequently that the voltage drops below 4V or even down to 0V, for times up to several seconds. Since it is impossible to buffer the voltage for such a long time we implemented a strategy called Brownout into GM8B Power control. The Basic idea behind this strategy is that if the voltage drops, the MAD gets an interrupt, saves the last state in the EEPROM, and shutsdown. When the Power is back the Brownout logic indicates to the software that a Power drop has happened, the software gets the data from the EEPROM, and resets the Brownout logic.

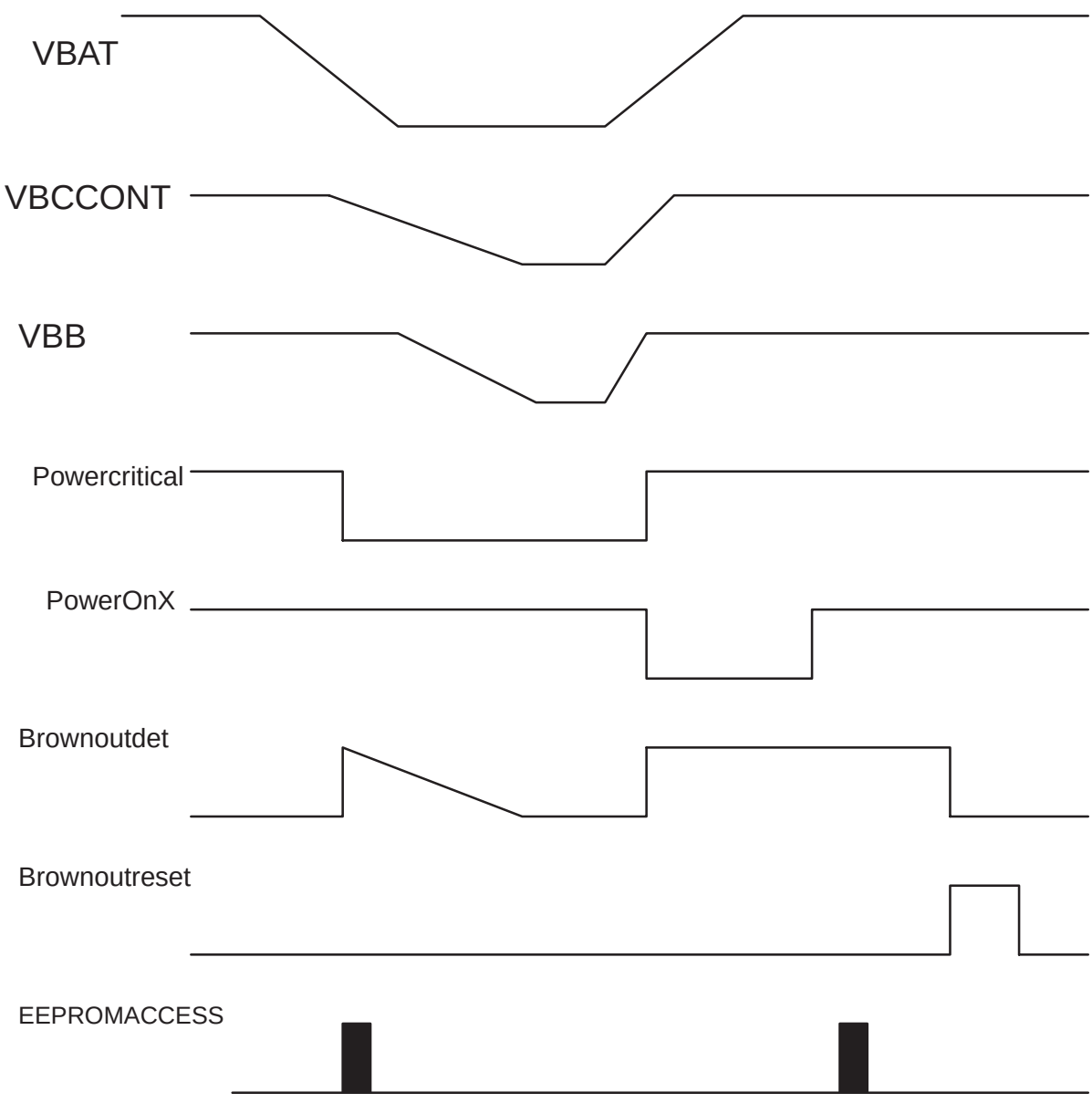


Figure 14. Brownout procedure total powerdrop

VDA Car Signals

Ignition sense

For GM8B, Ignition sense is an Input. This signal is turned high when the cars ignition is turned on, and low when the ignition is turned off again. The system behaviour regarding this signal is so that the phone is turned on, when Ignition is turned on, and turned off a programmable time after igntion is turned OFF

Table 13. Ignition sense

Parameter	max	typ	min	Notes
active voltage Ignition ON	16 V	13,5 V	9 V	
inactive voltage Ignition OFF	0,3 V		0 V	
Current taken from this signal	1 mA		10mA	
Maximum voltage in Fault condition	28 V 80V			for up to 60s for 500mS

Implementation

The Ignition sense Input is limited to 2.8V via an Resistor/ Z–Diode combination. The resuting signal is routed to a GENIO of the MAD, it is also a trigger signal for the wakeup logic.

Car Radio Mute

This signal is an output of CD949. It is an open collector output that is turned Low when a call is active.

Table 14. Antenna motor control

Parameter	max	typ	min	Notes
High voltage	16 V		9 V	No call active
Low voltage	0.3 V			call active
External pullup resistor		1 kΩ		
maximum drive current	150 mA			

The CRM implementation is reused from PHF–4, but is is not forfilling the Low–voltage requirement of 0.3V at the moment. But it is no real problem to make a version that forfills this specification.

Antenna Motor Control

This signal is an output of CD949. It is turned high when the phone ON and turned LOW when the phone is turned off

Table 15. Antenna motor control

Parameter	max	typ	min	Notes
Phone On	16 V		9V	
Phone Off	0.3V		0V	
drive current	100mA			

The Implementation of the AMC is completelly reused from DME–1D

Backlight Dimming

The Backlight dimming is used to synchronise the dimming of all backlights inside the cars cockpit. The Backlightdimming signal is a PWM modulated signal that is delivered from the car to the GM8B.

Table 16. Backlight dimming

Parameter	max	typ	min	Notes
High voltage	16V	13.5V	9V	
pulsewidth	100%		18%	for supplyvoltage < 13 V
pulsewidth	100%		13%	for supply voltage < 16 V
frequency	120 Hz		60 Hz	
Rise and fall times dV/dt dI/dt	200 mV/µs 20 mA/µS			

The Backlight dimming signal is inverted by an transisitor and then routed through an single gate inverter, to provide the following Lowpassfilter with an symetrical Push–Pull driver. The Lowpassfilter has a corner frequency of 0.1, to provide the ADC of the CCONT with the DC voltage that is proportional to the Dutycycle of the Backlight dimming signal. The information about the Duty cycle will be transfered as an M–Bus message to the Handset in order to dim the LEDs in the Handset.

When an unprogrammed module is powered up the first time the MCU starts from the boot rom inside the MAD2. The MBUS line is to be kept low to inform the MCU that the flash prommer is connected and the MCU should stop after the boot and wait for a download code.

When the flash programming is performed successfully the MCU switches to flash prom software. If the baseband is powered up for the first time the MCU will remain in local mode as the factory set has not been executed. To allow re–programming of working modules the MCU is at startup forced into local mode by connecting the MBUS to GND.

RF

Table 17. Main RF characteristics

Item	Values
Receive frequency range	935 ... 960 MHz
Transmit frequency range	890 ... 915 MHz
Duplex spacing	45 MHz
Channel spacing	200 kHz
Number of RF channels	124 (+50)
Power class	2 (39 dBm)
Number of power levels	18

Maximum Ratings

Nominal PA voltage:	**13.5V**
Lower extreme supply PA voltage:	10.5V
Higher extreme supply PA voltage:	16.5V
Nominal BB supply voltage is (CCONT) :	**2.80V**
Lower extreme voltage:	2.70V
Higher extreme voltage:	2.85V
Supply voltage for PA control logic:	**8.00V**
Lower extreme voltage:	7.60V
Higher extreme voltage:	8.40V
Supply voltage for charge pumps(CCONT) :	**5.00V**
Lower extreme voltage:	4.8V
Higher extreme voltage:	5.2V

Power Distribution

The following diagram shows the power distribution of the GM8B rf engine. All major rf modules are supplied with 2.85V from the BB ASIC CCONT. The specification of the regulators in the CCONT ASIC can be found in one of the following tables. In addition to this there is a dedicated 8V regulator for the supply of the PA control circuits as well as some buffer stages. The rf power amplifier itself is directly supplied by the car battery.

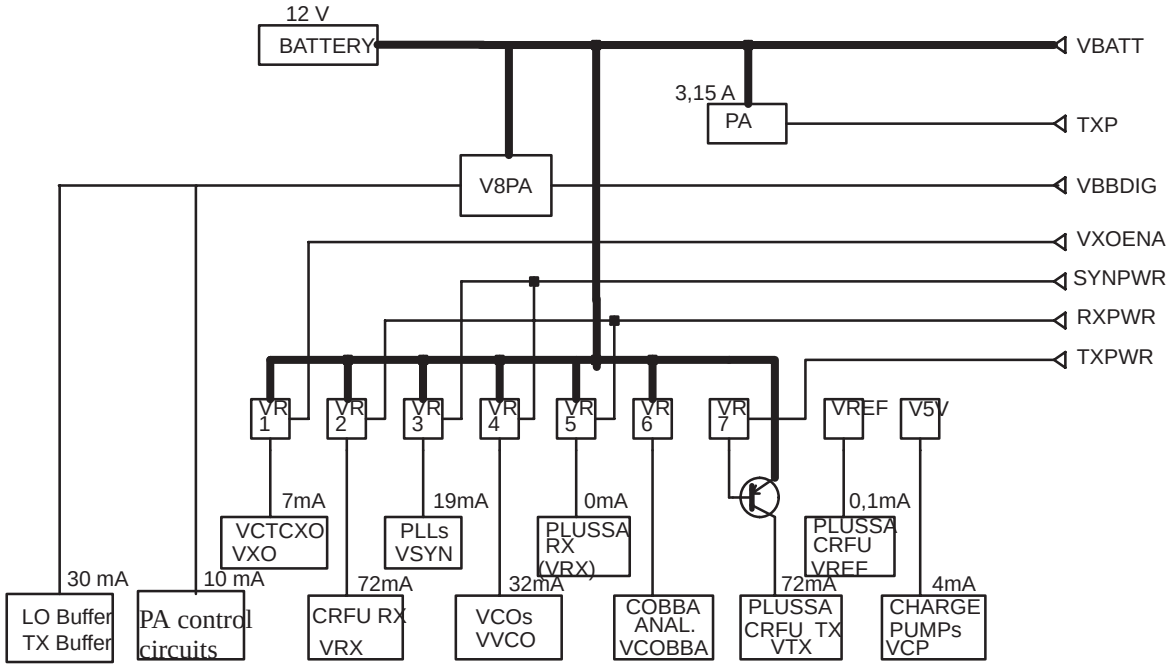


Figure 15. Power distribution diagram

Control Signals

Table 18. Control signals and typical current consumptions

VXOENA	SYNPWR	RXPWR	TXPWR	TXP	Typ. current cons.	Notes
L	L	L	L	L	<10 uA	Leakage current (PA)
H	L	L	L	L	7.0 mA	VCTCXO
H	H	L	L	L	60 mA	VCTCXO, VCOs, PLLs act.
H	H	H	L	L	130 mA	RX active
H	H	L	H	H	130 mA	TX active except PA
H	H	L	H	H	3280 mA	TX active, full power

All control signals are generated by MAD using 2.8 V logic.

Output Power

Table 19. List of supply voltages

Regulator in CCONT	Name of supply	Load	Current consumption
VR1	VXO	VCTCXO VCTCXO Buffer	2 mA 5 mA
VR 2	VRX1	LNA IF Amplifier	max. 25 mA max. 25 mA
VR 3	VSYN	Digital circuits off PLLs in PLUSSA	20 mA

Table 19. List of supply voltages (continued)

Regulator in CCONT	Name of supply	Load	Current consumption
VR 4	VVCO	UHFVCO VHFVCO CRFU 1a	10 mA 5 mA 7 mA
VR 5	VRX2	Plussa RX path	max. 32 mA
VR 6	VCOBBA	COBBA analog circuits	BB responsibility
VR 7	VTX	PLUSSA and CRFU 1a TX path	72 mA
V5V	VCP	Charge pumps in PLUSSA	4 mA
VREF	VREF	Reference voltage for CRFU1a and PLUSSA	
——	V8PA	TX buffer LO buffer Bias of detector diode OPAMPs for PA control	15 mA 15 mA 10 mA
——	VPA	Supply voltage PA	max. 4 A

Functional Description

The RF block diagram shows a conventional dual conversion receiver and the transmitter uses a single upconversion mixer. The architecture contains two RF ASICs, PLUSSA and CRFU1a.

CRFU1a is a BiCMOS circuit containing the LNA, RX mixer and TX mixer stages for the handportable GSM phones. However, in order to fulfill the specifications for the CD949 project a discrete LNA and a discrete RX mixer were employed.

PLUSSA is also a BiCMOS circuit which contains the IQ modulator for the transmitter and the receiver stages between the channel filter and COBBA. It also contains the PLLs for both the VHF and UHF synthesizers.

The Power amplifier is a MMIC (monolithic microwave integrated circuit) supplied by Hitachi. It has three amplifier stages including input and interstage matching.

Using the high integrated engine of DCT3 as much as possible reduces the component count. With this approach we want to fulfill the high demands for the reliability demands of the automotive industry.

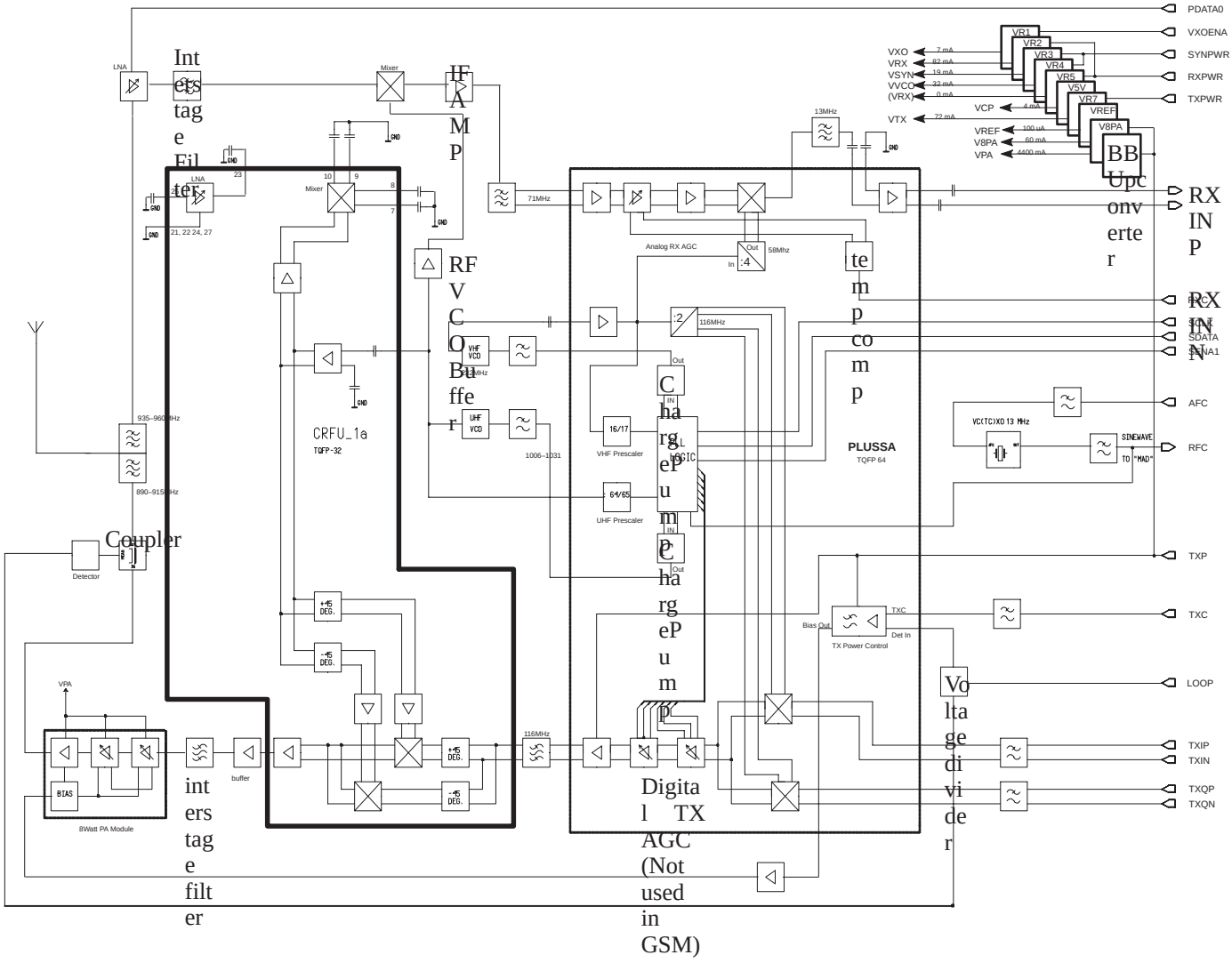


Figure 16. Block diagramm of the CD949 GSM RF part

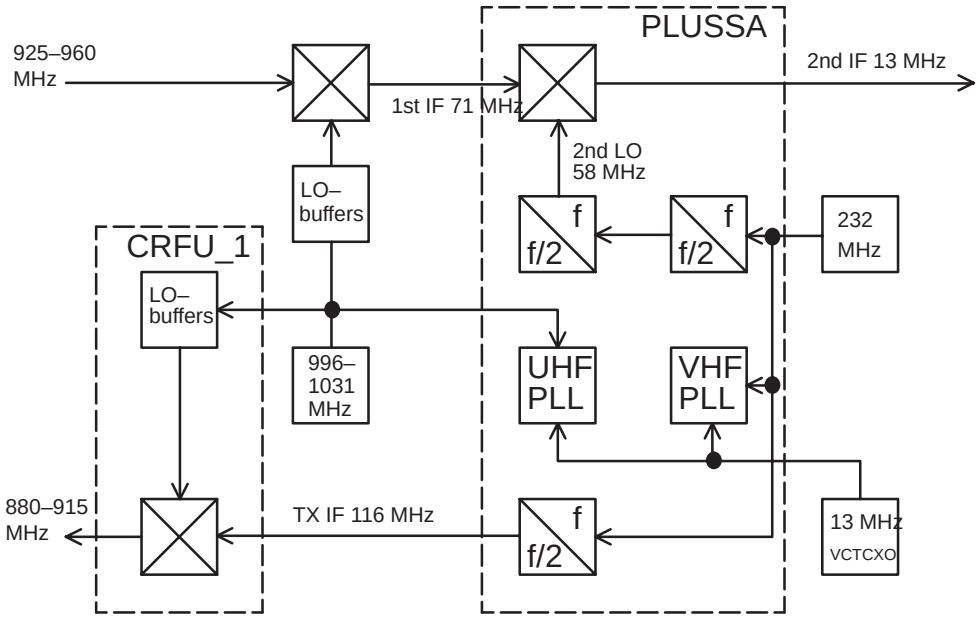


Figure 17. RF frequency plan

Receiver

The transceiver uses a dual conversion linear receiver. The received signal from the antenna is fed via the duplex filter to a discrete LNA (low noise amplifier) which uses a BFP420 transistor. The LNA can be switched between two gain settings in order to increase the dynamic range of the receiver. Switching of the LNA is controlled using the PDATA0 line from MAD using a discrete transistor network. The gain step in the LNA is activated when the RF input level at the antenna is less than –50 dBm.

Following the LNA, the signal is fed to the SAW interstage bandpass filter. This filter in combination with the helical duplex filter defines the spurious signal blocking for the receiver, in particular rejection of the image for mixing to the first RX IF frequency at 71 MHz.

The first mixer is a double balanced (quad diode hybrid) type. This is necessary in order to fulfill the strict blocking requirements, in particular the half IF rejection is critical. To provide the required gain an IF amplifier follows the mixer. Since the passive mixer requires a high LO signal level, additional local signal buffering is provided by a discrete buffer. The mixer uses upper sideband injection for generating the IF signal. The LO signal is generated with the UHF synthesizer.

The first IF signal is then channel filtered by a bandpass SAW filter with a bandwidth of ±100 KHz. It also provides attenuation to the image frequency for mixing to the second IF frequency (13MHz).

This filter also stops signals and mixing products at frequencies outside of the channel bandwidth from saturating proceeding amplifier stages, therefore reducing receiver sensitivity.

The next stage in the receiver chain is the AGC amplifier which is integrated into the PLUSSA ASIC. The control voltage for the AGC is generated by the DAC in the COBBA ASIC and provides a gain control range of 57 dB. The second mixer stage is also integrated into PLUSSA. The LO signal for the mixer stage is generated by dividing the VHF synthesizer frequency by a factor of four to produce 58 MHz. The resulting 2nd IF signal is at 13 MHz.

The 2nd IF filter is a ceramic bandpass filter located outside of PLUSSA. It is centered at 13 MHz with a bandwidth of ±100 KHz. The purpose of this filter is to attenuate signals at the adjacent channel frequencies except for the neighboring channels at ± 200 KHz which are filtered digitally by the DSP. The dynamic range of the DACs within COBBA is wide enough to cope with the effects of fading, particularly when the signal strength of the interferer is high.

After the 13 MHz filter there is a buffer stage in PLUSSA which converts the signal from single ended to differential to drive the DACs. The buffer has a voltage gain of 36 dB and the buffer gain setting in COBBA is 0 dB or 9.5 dB if required.

Transmitter

The transmitter chain contains an IQ–modulator, an upconversion mixer, a power amplifier and a power control loop.

The I and Q signals are generated by the DACs in COBBA in the BB section, post filtered (RC–network) and fed into the PLUSSA IQ modulator. The modulated IF signal from this modulator is centered at 116MHz (this is the VHF synthesizer frequency divided by two (232MHz)). Following the modulator, the signal is fed to a cascaded variable gain amplifier. It's gain is set to a fixed value of +4dB by a data word coming from the MCU in MAD. (This cascaded amplifier is used in other digital systems as well with stepped amplification values. PLUSSA is a core IC created to fulfill different standards and frequency concepts.) This first TX IF signal is then bandpass filtered and fed into the CRFU_1a. The TX part of this ASIC contains a double balanced Gilbert cell (which is an image rejection upconversion mixer), a buffer and two phase shifters for the LO signal. The CRFU_1a's output is single ended, therefore no external balun is necessary. The LO signal is generated by the UHF–synthesizer, fed into the phase shifters and then into the Gilbert cell.

The signal at the final TX frequency is then fed to a TX interstage filter, a buffer, a PA, a directional coupler, a duplex filter and and the antenna connector. The TX interstage filter is a bandpass type (dielectric or SAW filter) which attenuates the spurious signals of the upconverter and reduces the wideband noise of the signal. The buffer stage is used to provide the PA with sufficient input power. The final amplification is done by a Hitachi MosFet PA module. This module is internally matched to 50 ohm and is able to provide 20W of output power using an input level of approximately +3dBm. The power control range of this device is approximately 100dB.

The directional coupler is designed to measure the PA output power. The output power is detected by a detector diode and is used for the power control loop. A duplex filter provides sufficient TX/RX isolation and filters the harmonics generated by the PA.

Frequency Synthesizers

Both PLLs use the same reference signal generated by a13 MHz VCTCXO module (voltage controlled crystal oscillator). Temperature compensation is controlled by AFC (automatic frequency control). The VCTCXO frequency is adjusted using the signal received from the base station. AFC is generated by baseband with a 11 bit conventional DAC in COBBA.

PLUSSA contains the UHF PLL with prescaler, N, A and R dividers, phase detector and charge pumps. The prescaler is a dual modulus 64/65 (P/P+1) type and the charge pump supply current to the external loop filter. All PLL dividers are programmed via the 3–wire bus (i.e. SDATA, SCLK and SENA1).

The output signal of the prescaler is fed to N and A divider which produces one of the inputs to the phase detector.

The phase detector compares this signal with the reference signal divided by the reference divider from the VCTCXO. The error signal generated by the phase detector drives the charge pumps. The current pulses generated by the charge pumps are integrated by the loop filter to produce a control voltage for the UHF VCO. The settling time of the synthesizer is defined by the loop filter component values. The channel spacing is equal to the comparison frequency which is 200 KHz.

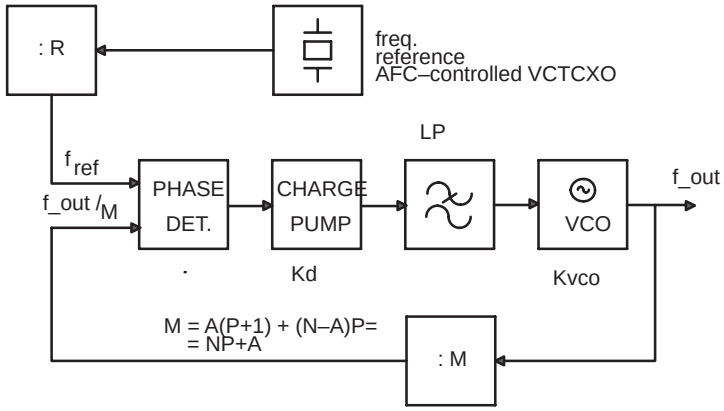


Figure 18. Phase locked loop , PLL

The VHF PLL is also located in PLUSSA. There is a 16/17 (P/P+1) dual modulus prescaler, N and A dividers, reference divider, phase detector and charge pumps. The VHF signal is generated by a discrete VCO circuit. The VHF PLL works in the same way as the UHF PLL. The VHF PLL operates at a fixed frequency (232 MHz) regardless of the traffic channel frequencies. A frequency divider is used after the VHF VCO in order to reduce phase noise.

Receiver Characteristics

RF Characteristics, Receiver

Table 20. Receiver characteristics

Item	Values
Type	Linear, FDMA/TDMA
IF frequencies	1st 71 MHz, 2nd 13 MHz
LO frequencies	1st LO 1006 ... 1031 MHz, 2nd LO 58 MHz
Typical 3 dB bandwidth (reference noise band-width)	+/– 90kHz
Sensitivity	min. – 104 dBm , S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	88 dB
Receiver output level (RF level –104 dBm)	50 mVpp (typical balanced signal level of 13 MHzIF in RF BB interface = input level to RX ADCs)
Typical AGC dynamic range	50 dB
Accurate AGC control range	57 dB

Table 20. Receiver characteristics (continued)

Item	Values
Typical AGC step in LNA	approx. 45 dB
Usable input dynamic range	–104 ... –10 dBm
RSSI dynamic range	–112 ... –48 dBm
AGC relative accuracy on channel (accurate range)	+/– 0.8 dB
Compensated gain variation in receiving band	+/– 1.0 dB

Receiver Module Specification

Duplex filter

Table 21. Duplex filter specification

Parameter	Transmit section		Receive section		unit
Center frequency, ftx,frx	ftx : 902.5		frx : 947.5		MHz
BW (bandwidth) at passband	+/– 12.5		+/– 12.5		MHz
Maximum insertion loss at BW	1.5		2.8		dB
Minimum insertion loss	0.3		–		dB
Ripple at BW, peak to peak	1.0		1.0		dB
Terminating impedance	50		50		ohms
min. input/output matching Mag(S_{11}) and Mag(S_{22})	–11		–11		dB
Minimum attenuations	Freq.range	Att.	Freq.range	Att.	
	640 ... 820	20	0...800	35	MHz/dB
	925 ... 940	30	890...915	15	MHz/dB
	940 ... 960	30	980...1050	15	MHz/dB
	960 ... 976	10	1067...1102	35	MHz/dB
	1574 ... 1577	25	1102...2000	25	MHz/dB
	1760 ... 1830	30	2000...3500	30	MHz/dB
	2640 ... 2745	30			MHz/dB
	3520 ... 3660	30			MHz/dB
Permissible input power	4 AVG				W
Temperature Range	–35 ... 85		–35 ... 85		deg Cel

Pre–amplifier Specifications

The LNA is a discrete solution using a BFP420 as active component.

Table 22. LNA requirements

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency band		935 – 960		MHz
Supply voltage	2.7	2.8	2.855	V
Current consumption			25	mA
Insertion gain Mag(S_{21})	19	20	21	dB
Noise figure		1.8	2.0	dB,PDATA0=H
IIP3	–2			dBm, PDATA0=H
Input 1 dB compression point	–12			dBm, PDATA0=H
Reverse isolation Mag(S_{12})	25			dB
Input matching Mag(S_{11})	–7			dB
Output matching Mag(S_{22})	–10			dB
Gain reduction	35		40	dB,room temp.
Step accuracy	–2		+2	dB,over temp.range
Noise figure, when PDATA=0			25	dB

RX Interstage Filter

Table 23. RX interstage filter requirements

Parameter	Min.	Typ.	Max.	Unit
Passband		935 – 960		MHz
Insertion loss			4.0	dB
Ripple in passband			1.0	dB
Attenuation DC...890 MHz	35			dB
Attenuation 890...915 MHz	15			dB
Attenuation 980...1030 MHz	15			dB
Attenuation 1067...1102 MHz	35			dB
Attenuation 1102...1500 MHz	30			dB
Terminating impedance		50		ohm
Input matching Mag(S_{11})	–9.5		–9.5	dB
Maximum drive level			+10	dBm

Diode Mixer Specification

The 1st mixer will be a passive quad diode hybrid as it was used in CD745.

Table 24. Mixer requirements

Parameter	Min.	Typ./ Nom.	Max.	Unit/Notes
RX frequency range	935		960	MHz
LO frequency range	1006		1031	MHz
LO drive level	+6			dBm
IF frequency		71		MHz
Conversion gain		–7		dB
NF, SSB		7		dB
IIP3	+13			dBm
1 dB Compression Point	+3			dBm
IF/2 spurious rejection	67			dBm, *
LO power level in RF–port			–25	dBm
Input matching Mag(S_{11})			–9.5	dB
Impedance		50		ohm

IF Amplifier Specification

Table 25. Electrical characteristics

Parameter	min.	typ.	max.	unit
Operating temperature range	–30		+85	deg.C
Supply Voltage	2.7	2.8	2.85	
Current Consumption		22	25	mA
Center frequency , fo		71		MHz
Insertion Gain	21	22	23	dB
Noise figure		2	3	dB
IIP3	–1			dBm
1dB Input Compression Point	–11			dBm
In– / Output matching		50		ohm

IF Filter Specification

Table 26. Electrical characteristics

Parameter	min.	typ.	max.	unit
Operating temperature range	–30		+85	deg.C
Center frequency , fo		71		MHz
Maximum ins. loss at 1dBBW			11	dB
Group delay ripple at 1dBBW			1.3	us pp

Table 26. (continued) Electrical characteristics

Parameter	min.	typ.	max.	unit
Bandwidth relative to 71 MHz 1 dB bandwidth 3 dB bandwidth 5 dB bandwidth 22 dB bandwidth 30 dB bandwidth 40 dB bandwidth	 +/– 90 +/–120		 +/– 230 +/– 350 +/– 550 +/– 700	kHz
Spurious rejection, fo +/– 26 MHz	65			dB, *
Terminating impedance (balanced) resistance capacitance (parallel)		2k||10p		kohm||pF

CRFRT RX Part Specification

In CD949 the IF backend is build around the DCT3 ASIC Plussa. Also an additional 13 MHz filter is used. The specification of this filter is also added into this chapter.

Table 27. AGC and 2nd mixer in PLUSSA, requirements

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
Current consumption (VRX)			32	mA
Input frequency range	45		120	MHz
2nd IF frequency range	0.4		17	MHz
Total noise figure, SSB, max. gain			15	dB
Total noise figure, SSB, min. gain			65	dB
Max. voltage gain	40			dB
Min. voltage gain			–17	dB
Control voltage for min. gain		0.5		V
Control voltage for max. gain		1.4		V
Output 1 dB compression point @ max. gain	800			mVpp
Input 1 dB compression point @ min. gain	80			mVpp
IF input impedance (balanced)	2.4/tbd	3.8/2	5.6/tbd	kohm/pF
2nd mixer output impedance (single output)			100	ohm

Table 28. 2nd IF–filter connected to PLUSSA

Parameter	min.	typ.	max.	unit
Center frequency, fo		13		MHz
1 dB bandwidth, 1 dBBW (relative to 13 MHz)	+/– 90			kHz
Insertion loss			8.0	dB
Amplitude ripple at 1 dBBW			1.0	dB
Group delay ripple at 1 dB BW, peak to peak			1.5	us
Attenuations, relative to 13 MHz fo +/– 400 kHz fo +/– 600 kHz fo +/– 800 kHz	 25 35 35			dB

Transmitter Characteristics

RF Characteristics, Transmitter

Table 29. Transmitter characteristics

Item	Values
Type	Upconversion, nonlinear, FDMA/TDMA
Intermediate frequency (phase modulated)	116 MHz
LO frequency range	1006 ... 1031 MHz
Max. Output power	8 W peak
Gain control range	min. 34 dB
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

Table 30. Output power requirements

Parameter	Min.	Typ.	Max.	Unit / Notes
Max. output power		39.0		dBm
Max. output power tolerance (power level 2)			+/– 2.0 +/– 2.5	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 3...15			+/– 3.0 +/– 4.0	dB, normal cond. dB, extreme cond.
Output power tolerance / power levels 16...19			+/– 5.0 +/– 6.0	dB, normal cond. dB, extreme cond.
Output power control step size	0.5	2.0	3.5	dB

Sub Block Description/Tables

Electrical Specifications, CRFRT TX Section

In the CD949 rf module the modulator is integrated into the DCT3 ASIC Plussa.

Table 31. Requirements for IQ–modulator

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Current consumption (VTX)		28	tbd.	mA
Modulator Inputs (I/Q)	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Input bias current (balanced)			100	nA
Input common mode voltage		0.8		V
Input level (balanced)			1.2	Vpp
Input frequency range	0		300	kHz
Input resistance (balanced)	200			ohms
Input capacitance (balanced)			4	pF
IQ–input phase balance total, temperature included	–4		4	deg.
IQ–input phase balance temperature effect	–2		2	deg.
IQ–input amplitude balance total, temperature included	–0.5		0.5	dB
IQ–input amplitude balance temperature effect	–0.2		0.2	dB
Modulator Output	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Output frequency	85		400	MHz
Available linear RF power into 100 ohm balanced load	–9	–7		dBm
Available saturated RF power into 100 ohm balanced load (max. gain in AGC)	–5	–3		dBm
Noise level in output			–145	dBm/Hz avg.
Total gain		4		dB

The modulated TX signal is centered at 116MHz. Following the modulator this signal is fed through an discrete filter to suppress any high frequency harmonics.

Table 32. 116 MHz LC IF–filter, requirements

Parameter	Min.	Typ.	Max.	Unit
Center frequency		116		MHz
Insertion loss @ 116 MHz			3.0	dB
Relative attenuation @ +/– 10 MHz offset	5			dB

Table 32. 116 MHz LC IF–filter, requirements (continued)

Parameter	Min.	Typ.	Max.	Unit
Relative attenuation @ +/– 20 MHz offset	8			dB
Relative attenuation @ 232 MHz	15			dB
Relative attenuation @ 348 MHz	20			dB
Relative attenuation @ 464–1000 MHz	25			dB
Input impedance, balanced		100		ohm
Output impedance, balanced		200		ohm

Mixer Specification

Table 33. Requirements for the upconversion mixer in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	2.7	2.8	2.85	V
Supply current			50	mA
Input frequency		116		MHz
Input level	–8	–5		dBm
Output frequency range	890		915	MHz
Output level	+3	+5		dBm
NF,SSB			20	dB
LO–signal level in output			–29	dBc
Unwanted sideband level			–15	dBc
fLO+/–2xIF spurious level			–40	dBc
7x116 MHz spurious level			–40	dBc
8x116 MHz spurious level			–55	dBc
Input impedance (balanced)		200//tbd.		ohm//pF
Output matching Mag(S_{22}) (with matching network)			–9.5	dB

TX Filter Specifications

Table 34. Specification TX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	890 – 915			MHz
Insertion loss			3.5	dB
Ripple in passband			1.5	dB
Attenuation DC...813 MHz	30			dB
Attenuation 925...935 MHz	4.5*			dB
Attenuation 935...960 MHz	5**			dB
Attenuation 1006...1031 MHz	40			dB
Attenuation 1122...1147 MHz	30			dB
Attenuation 1780...1830 MHz	10			dB
Attenuation 2670...2745 MHz	10			dB
Terminating impedance	50			ohm
Input/Output matching Mag(S_{11}) Mag(S_{22})			–8	dB
Maximum drive level			+10	dBm

Power Amplifier

Table 35. Specification MosFet power amplifier Tamb = +25 deg. C, 50 ohms

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			890		915	MHz
Supply voltage			10.5	12.5	16.5	V
Current consumption, extreme conditions		Pout=41.5dBm, V_{DD}=10.5V			4.5	A peak
Current consumption, nominal conditions		Pout=41.5dBm, V_{DD}=13V		3.15	3.65	A peak
Input power	Pin			3	13	dBm
Output power 1	Pout 1	Pin= 3 dBm, V_{DD}=12.5 V, Vapc=7 V, Tc=+25 deg.C	42.3	43.6		dBm
Output power 2	Pout 2	Pin= 3 dBm, V_{DD}=10.3 V, Vapc=7 V, Tc=+80 deg.C	39.5	40.8		dBm
Power control range		Vapc= 2 ... 7 V		100		dB
Isolation		Pin= 3 dBm, V_{DD}=12.5 V, Vapc=0.5 V, Tc=+25 deg.C		–60	–40	dBm
Carrier switching time	tr, tf	V_{DD}=12.5 V, Pin=3 dBm Pout= 13W		1.5	2	us
Total efficiency		Pin= 3 dBm , Pout= +41.1 dBm, V_{DD}=12.5 V	30	35		%
Control current	Iapc			0.9		mA peak
Harmonics, 2nd				–50	–40	dBc
Harmonics, 3rd				–55	–45	dBc

Table 35. Specification MosFet power amplifier (continued) Tamb = +25 deg. C, 50 ohms

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Input matching Mag(S_{11})				–9.5	–6.0	dB
Operating case temperature			–30		+110	°C
storage temperature			–40		+110	°C
APC voltage	Vapc		0		8	V
Duty cycle		Pout=41.5dBm, V_{DD}=10.5V Pin= 3 dBm, Tc=+25 deg.C	50			%
Stability Load mismatch stress		Pin= 3 dBm, V_{DD}=12.5 V, Load VSWR 20:1, all phases	no parasitic oscillation			

Power Control Circuit

Table 36. Directional coupler characteristics

Parameter	Min.	Typ.	Max.	Unit/Notes
Frequency range	890		915	MHz
Insertion loss			0.4	dB
Coupling factor		20		dB
Directivity		30		dB
Impedance level of the main line		50		ohm
Matching main line Mag(S_{11}) and Mag(S_{22})		–20		dB
Impedance level of the coupled line		100		ohm

Table 37. Specification of the Power Detector

Parameter	Test condition	Min	Typ	Max	Unit
Freq. Range		890		915	MHz
InputPower	Power Level 19 – 2	–13		21	dBm
Linear range					
Dynamic range					
Output Voltage	Low Power Mode	tbd (1.65)		tbd (2.0)	V
Output Voltage	High Power Mode	tbd (1.65)		tbd (3.6)	V
Supply Voltage		7.6	8	8.4	V
Supply current					
Temperature Drift			tbd		mV

Table 38. Dual range power control loop characteristics

Parameter	High power loop	Low power loop
Power level	2 ... 10	11 ... 19
DET voltage	200mV ... 1250mV	250mV ... 1580mV
LOOP amplification factor	0.5	5
Bias voltage for PA	2V ... 7V	1.7V ... 2V

Table 39. Dual range power control loop characteristics

Parameter	High power loop	Low power loop
Power level	2 ... 10	11 ... 19
DET voltage	200mV ... 1250mV	250mV ... 1580mV
LOOP amplification factor	0.5	5
Bias voltage for PA	2V ... 7V	1.7V ... 2V

Table 40. Specification of the TXC Offset shifter

Parameter	Test condition	Min	Typ	Max	Unit
Supply Voltage		7.6	8V	8.4	V
Min output voltage			tbd 1.2		V
Max output voltage	Low Power Mode		tbd 2.3		V
Max output voltage	High Power Mode		tbd 4.2	7	V
Temperature drift	from –20¿C to +80¿C, depends on 8V temp. drift		tbd		mV

Table 41. Specification of the Error amplifier

Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage		7.6	8.0	8.4	V
Min output voltage	MC 33074 @ 5V	–	0.1	0.3	V
Max output voltage	MC 33074 @ 5V	3.7	4.0	–	V
Gain			tbd (15)		1
fc			tbd (35)		kHz
Temperature drift	from –20¿C to +80¿C		tbd (0)		mV

Synthesizer

VCTCXO

Table 42. Electrical specifications

Parameter	Min.	Typ.	Max	Unit/.Notes
Supply voltage, Vcc	2.70	2.80	2.90	V
Current consumption, Icc			1.5	mA
Operating temperature range	–30		+85	deg. C
Nominal frequency		13		MHz
Output voltage swing (swing of 13 MHz component, selective measurement from the spectrum)	800			mVpp
Load, resistance capacitance		2 10		kohm pF
Frequency tolerance @+25 deg. C	– 1.0		+ 1.0	ppm
Frequency tolerance after reflow (@ +25 deg. C)	– 2.0		+ 2.0	ppm
Frequency stability vs. temperature (ref. @+25 , –30....+85 deg. C)	– 5.0		+ 5.0	ppm
Frequency stability vs. supply voltage (2.8 V +/– 100 mV)	– 0.1		+ 0.1	ppm
Frequency stability vs. load change (2 kohm//10 pF +/– 10 %)	– 0.3		+ 0.3	ppm
Aging	– 1.0		+ 1.0	ppm/year
Nominal control voltage, Vc		1.3		V
Voltage control range	0.3		2.3	V
Voltage control characteristics (see note 1.)	+/– 14		+/– 20	ppm/V when 0.3 V<Vc<2.3 V
Vc input resistance	1			Mohm
Frequency adjustment	+/– 3.0			ppm with inter–nal trimmer
Harmonics (with 2 kohm//10 pF)			– 5	dBc
Start up time output level within 90% output frequency limits +/–0.5ppm from the final value			4.5	ms
Phase noise @ 1 kHz offset			–130	dBc/Hz

VHF VCO + Filter

Table 43. VHF VCO requirements

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage range	2.7	2.8	2.9	V
Current consumption			7	mA
Control voltage	0.5		4.0	V
Operation frequency		232		MHz
Output level	–13	–10		dBm (output after low pass filter)
Harmonics			–30	dBc, (filtered)
Phase noise, fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz			 –123 –133 –143	dBc/Hz
Control voltage sensitivity	8.0		16.0	MHz/V
Pushing figure			+/– 2	MHz/V
Frequency stability			+/– 3	MHz (over temperature range –30...+85 C deg.)
Spurious content			–70	dBc

UHF PPLL

Table 44. UHF–synthesizer, requirements

Parameter	Min.	Typ.	Max.	Unit/Notes
Start up settling time			3.0	ms
Settling time +/– 25 MHz		500	800	us, (into +/– 20 Hz from final frequency)
Phase error			3.7	deg./rms
Sidebands +/– 200 kHz +/– 400 kHz +/– 600...+/–1400 kHz +/–1.4... +/– 3.0 MHz > +/– 3.0 MHz			 –40 –60 –66 –76 –86	dBc

UHF VCO

Table 45. UHF VCO module, Electrical specifications, Zo=50 ohm

Parameter	Conditions	Rating	Unit/ Notes
Supply voltage, Vcc		2.8 +/– 0.1	V
Supply current, Icc	Vcc = 2.8 V, Vc= 2.25 V	< 10	mA
Control voltage, Vc	Vcc = 2.8 V	0.8... 3.7	V
Oscillation frequency	Vcc = 2.8 V Vc = 0.8 V Vc = 3.7 V	 < 1006 > 1031	 MHz MHz

Table 45. (continued) UHF VCO module, Electrical specifications, Zo=50 ohm

Parameter	Conditions	Rating	Unit/ Notes
Tuning voltage in center frequency	f = 1013.5 MHz	2.25 +/– 0.25	V
Tuning voltage sensitivity in operating frequency range on each spot freq.	Vcc = 2.8 V f=1006...1031 MHz	16+/– 2	MHz/V
Output power level	Vcc=2.7 V f=1006...1031 MHz	–6.0 min.	dBm
Output impedance and VSWR	f=1006...1031 MHz	50 ohms,VSWR <2	
Phase noise, fo +/– 25 kHz fo +/– 600 kHz fo +/– 1600 kHz fo +/– 3000 kHz	Vcc=2.8 V f=1006...1031 MHz	–100 –120 –130 –140	dBc/Hz max.
Pulling figure	VSWR=2, any phase	+/– 1.0	MHz max.
Pushing figure	Vcc=2.8 +/– 0.1 V	+/– 2.0	MHz/V max.
Frequency stability over temperature range	Ta=–30 ... +85 deg. C	+/– 3.0	MHz max.
Harmonics		–10 max.	dBc
Spurious	Vcc=2.8 V, Vc=0...6 V	–70 max.	dBc
Input capacitance in Vc–pin	Vc= 0 V	100 max.	pF

UHF VCO Buffer

Table 46. Buffer for RX downconverter

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage	7.8	8.0	8.2	V
Supply current		15		mA
Frequency range	1006		1031	MHz
Input power			–6	dBm
Output power	6			dBm
1 dB input compression		–7		dBm
IIP3		+3		dBm
Harmonics		–45		dBc

The RX LO buffer is a discrete realization and amplifies the UHF LO signal to the level required by the RX mixer.

Table 47. UHF local signal input in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Input frequency range	990		1040	MHz
Input level	200		700	mVpp
Input resistance		100		ohm
Input capacitance			1.5	pF

PLL Circuit

Table 48. UHF PLL block in PLUSSA, requirements

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	650		1700	MHz
Input signal level (f<1.5 GHz)	200			mVpp
Input resistance	600	700		Ohm
Input capacitance		1.8	3	pF
Supply current		10	12	mA
Reference input frequency			13	MHz
Reference input impedance	10||1			kΩ ||pF
Phase comparison frequency			1	MHz
Charge pump output current 1 current 2		0.5 2.0		mA
Sink to source current matching error of the charge pump			+/– 5	%
Charge pump current error			+/– 10	%
Charge pump current temperature variation			+/– 10	%
Charge pump leakage current			5	nA
Phase detector phase noise level			–163	dBc/Hz

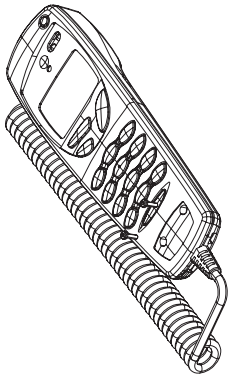
Antenna

In CD949 the responsibility for the antenna is at the customer. The CD949 project responsiblility ends at the RF connector (MINI–UHF type). The impedance at this point is 50 Ohm. The antenna connection itself is designed to withstand 16.5V DC. This is achieved by DC decoupling by a simple capacitor in series to the rf input.

Antenna Specification

There is no antenna specification for the CD949 antenna. Any standard active or passive GSM antenna should work together with CD949.

Handset (RTE–2HJ)



Power up/Power down procedure HS

This task is divided up between hard– and software to protect accidential power down of SIM. As long, ”+5V” is below 4.63V, Reset is active (active LOW, Net: _RESOUT), and min. 20msec after 4.63V was reached. After _RESET is high, software has to wait in a loop until Net: ”SUPPLYOK” goes high. This is at the point, where the Voltage supplied via Cable is over 7 Volt. After this happens, HS–Microcontroller can start the normal program (with SIM–start). If Voltage supplied via Cable goes below 6.2 Volts, the microcontroller is interupted via ”SUPPLOWIRQ” (active low), then it must be monitored. If it is low for a certain time, the system has to be shut down. This shut down should terminate in the wait loop from the beginning (until SUPPLYOK).

The HS will be connected with a 10 pol RJ45 connector to the cabletree which is going to the RU.

On the HS PCB there is a 1*10 pol male right angle connector typ SMK CGP4710–0101 to connect the curly cord to the HS.

D.C. Characteristics

Supply Voltage

To supply the HS different voltages are needed, they are generated from the 8V supply of the RU. In the HS there are regulators for generating stabilized 5V and 3V. The following figure shows the power distribution inside the HS.

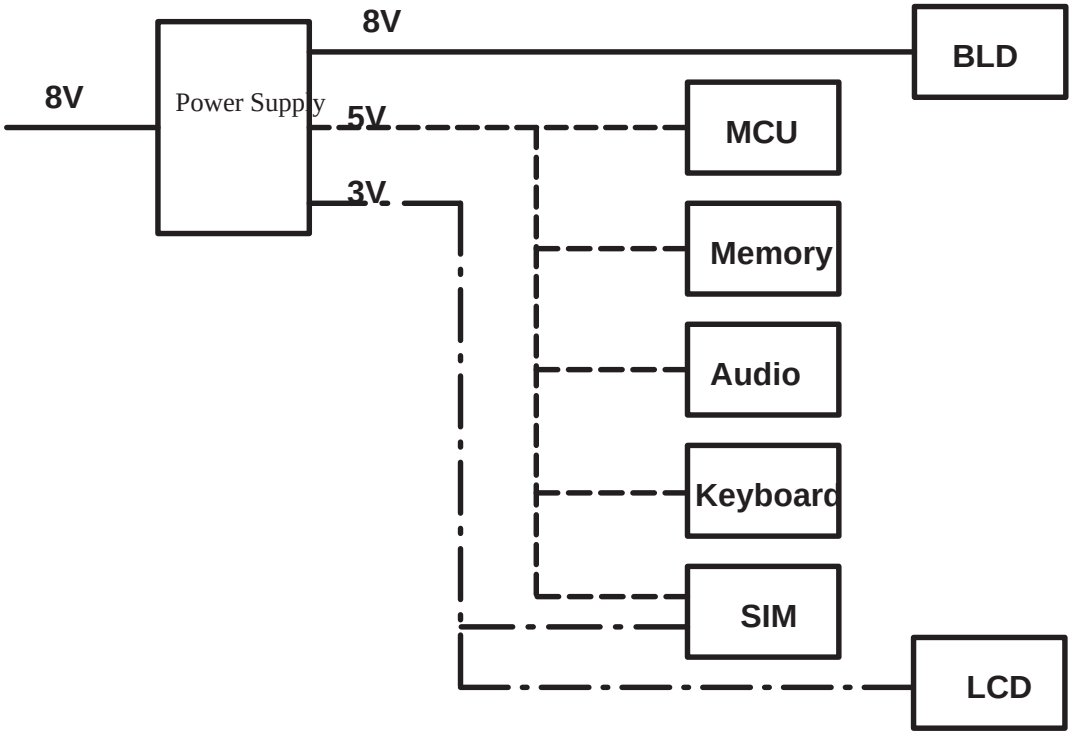


Figure 19. Power distribution diagram

Reset strategy is divided up between hard– and software to protect accidential power down of SIM. As long, ”+5V” is below 4.63V, Reset is active (active LOW, Net: _RESOUT), and min. 20msec after 4.63V was reached. After _RESET is high, software has to wait in a loop until Net: ”SUPPLYOK” goes high. This is at the point, where the Voltage supplied via Cable is over 7,0 Volt. After this happens, HS–Microcontroller can start the normal program (with SIM–start).

If Voltage supplied via Cable goes below 6.0 Volts, the microcontroller is interupted via ”SUPPLOWIRQ” (active low), then it must be monitored. If it is low for a certain time, the system has to be shut down. This shut down should terminate in the wait loop from the beginning (until SUPPLYOK).

Current Consumption

The handset current consumption dependents on three different parts:

1. digital part
2. backlight diming
3. audio

If only the digital part is active (no call active and BLD is switched offf) the current consumption is around 40 mA. When BLD is switched on with a duty cycle of 100% the current consumption is increased to approximately 90 mA. Depending on the BLD duty cycle the current consumption is varying between 40 mA and 90 mA. If a call is active the current consumtion can increase up to 100 mA when BLD duty cycle is 100%

External Signals and Connections

The handset is connected via curly cord to the system cable and then to the RU. The curly cord uses an 10 pol western plug which will be connected to the system cable.

HS Module Connector

Table 49. Handset connector

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	N.C.				not connected / HS side =GND
2	MBUS	0 2.0	 9600	0.8 2.8 5 5	V / low voltage V / high voltage µs / risetime µs / falltime baud/ transmission rate
3	+8V	7,2	8,0	8,8 100	V / supply voltage mA / supply current
4	GND				ground from RU
5	HSEARP		17,5	501	mV / earpiece + to earpiece –
6	HSEARN		17,5	501	mV / earpiece – to earpiece +
7	PWR_ON	 3.6		0.7 3.8	V / low voltage V / high voltage
8	HSMICP		87	790	mV / microphone + to microphone –
9	HSMICN		87	790	mV / microphone – to microphone +
10	N.C.				not connected / HS side =GND

Pins 1 and 10 are connected to ground in HS for EMC protection purposes and not connected in RU/ SCM–5.

Functional Description

Power On Key

Power ON/OFF key is connected to the RU via a seperate line. If the DC level,delivered from the RU, is switched to ground the CCONT in the RU detect this as power up of the system and switches on RU and HS.

Keypad Switch Matrix

Keyboard is held in SIMPLEX style. Keys are arranged in 4*4 matrix structure and activities will generate an interrupt. The 4 horizontal rows are routed to an input port of the MCU and the 4 vertical columns are routed to an output port of the MCU. After reception of the keyboard interrupt the SW can determine exactly which key was pressed.

LCD Module

As display a passive, full dot matrix (48*84) Liquid Crystal Display module in foil compensated super twisted nematic technology with integrated driver from Phillips will be used. Size of the display is 39.5*34*3.5 mm. The LCD display is working with 3V instead of 5V for the MCU and therefore a level–shifter is needed between MCU and LCD display. Data to be displayed will be transfered via a serial communication interface from the MCU to the LCD display.

Back Light

The Back Light Dimming circuit is used to illuminate the keyboard and LCD–Display depending from the backlight dimming signal of the car (Kl.58g). For the HS only yellow green LEDs are used. Inside the RU a MBUS message is generated and sent to the HS. The MCU of the HS will then generate two PWM signals to control the back light dimming circuit. Two PWM signals are generated to have the chance to illuminate keyboard and LCD–Display in different ways if necessary. The LEDs are driven by two constant current sources.

Mic/Speaker

As microphone an electret condenser microphone from Matsushita typ WM–66EC110 will be used. The diameter of the microphone is 6mm.

The microphone signal is bandwidth limited and amplified and routed as balanced signal to the RU. The needed reference voltage for biasing of the OPs will be generated by an OP voltage follower out of the 5V supply voltage. Also this 2.5V voltage is used for biasing of the microphone and the microphone amplifier.

The balanced earpiece signal from the RU is bandwidth limited and amplified and then routed thru the earpiece.

A Phillips earpiece typ WD 00918/32U will be used. The diameter is 23 mm.

HOOK Detection

For detection if the HS is inside or outside the cradle a hall detector is used. The cradle contains there a permanent magnet, so if the HS is inside the cradle the switch of the hall detector is closed and hook line is connected to GND. The Hook line then goes to an interrupt input of the MCU.

MBUS

The bidirectional MBUS between RU and HS is working at 2.8V. Inside the HS the bidirectional MBUS is split into TX and RX direction and then fed to one of the serial communication interfaces of the MCU. The split circuit makes also the level shift from 2.8V to 5V which is needed by the MCU. The prefered bit rate will be 9600 bit/s but can be speeded up to 19.2 kbit/s if needed by the SW to refresh the LCD display in a sufficient time. (not needed at the moment, due to successful compression work of the SW group)

Memory

The HS has no external FLASH or MASK ROM memory on board so the ROM is limited to the 128k*8 of the MCU. External RAM (32k*8) is connected to the MCU.

Cradle (CRD–8))

System Description

The cradle can be used for left and right hand cars and will fit physically into the cars of MB, Audi and Ford. It will be used together with the Minna Handset and with the Dude Handset, both handsets having the same mechanical interface. The Minna HS has an emergency button; the Dude HS has no emergency button.

Otherwise the HS's are equal from the mechanical point of view. The cradle offers the following functionality:

–Locking/release mechanism

–Switch between Hands–free and private mode supported through a magnet

There is no PCB inside the Cradle and no illumination of the push buttons.

Cradle Concept

The mechanical concept of the cradle is based on the DCT3 cradles and uses a similar locking/release mechanism. The DCT3 cradle uses one spring for the whole locking/release mechanism making assembly easier. The cradle is designed so that the user has easy access to the locking/release mechanism when used either on dashboard or armrest mounting.

No.	Acc.	Characteristics	Specification
1		Main Dimensions	94 mm (L) x 71mm (W) x 34mm (H)
2		Weight	60g
3		Materials	Housing: PC/ABS Push Buttons: POM Slider: PA + GF
4		PCB	No PCB
5		Shielding	No Shielding
6		Mounting	Dashboard & Armrest
7		Mounting Plate	CRD–8 Mounting plate or Swivel Mounting Plate
8		Fixation	Screwed
9		Screw Pattern	35mm x 38mm 17,5mm (2 screws) 24,5mm (2 screws)
9		HS Release Button	2
10		Button Illumination	No
11		Hook Detection	Permanent magnet
12		IP Class	IP5K0 with Handset in a mounted position IP 30 the cradle
13		Colour	Nokia warm black
14		Surface Structure	According VDI3400 Ref. 30
15		Temperature Range	–40°C…+85°C
16		Mechanical Requirements	CD940 Specification.
17		General Mechanical Requirements	NMP SPR 3&4 Car industry req.